

Circle 520

# High-Voltage Power Pulse Circuit

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**F**ast rise-time high-voltage pulses have many uses ranging from EMC testing to device characterization. The simple, low-cost circuit described here deals with the latter. It's able to generate 0- to 1000-V pulses with currents up to 50 A, and a rise time of 100 ns for 800 V/30 A. The output can withstand short circuits, and capacitive and inductive loads. Pulse length and repetition rate are determined by an optically isolated TTL-input signal. Commercial equipment like pulse/function generators or a PC can be connected to this input. The pulse's amplitude is set by the HV supply; a low-cost photomultiplier-type supply (0, 5 .5 mA) can be used when repetition rates are below 20 Hz.

The circuit operates as follows: when applying the HV supply, C1 is charged up to a voltage HV via R1

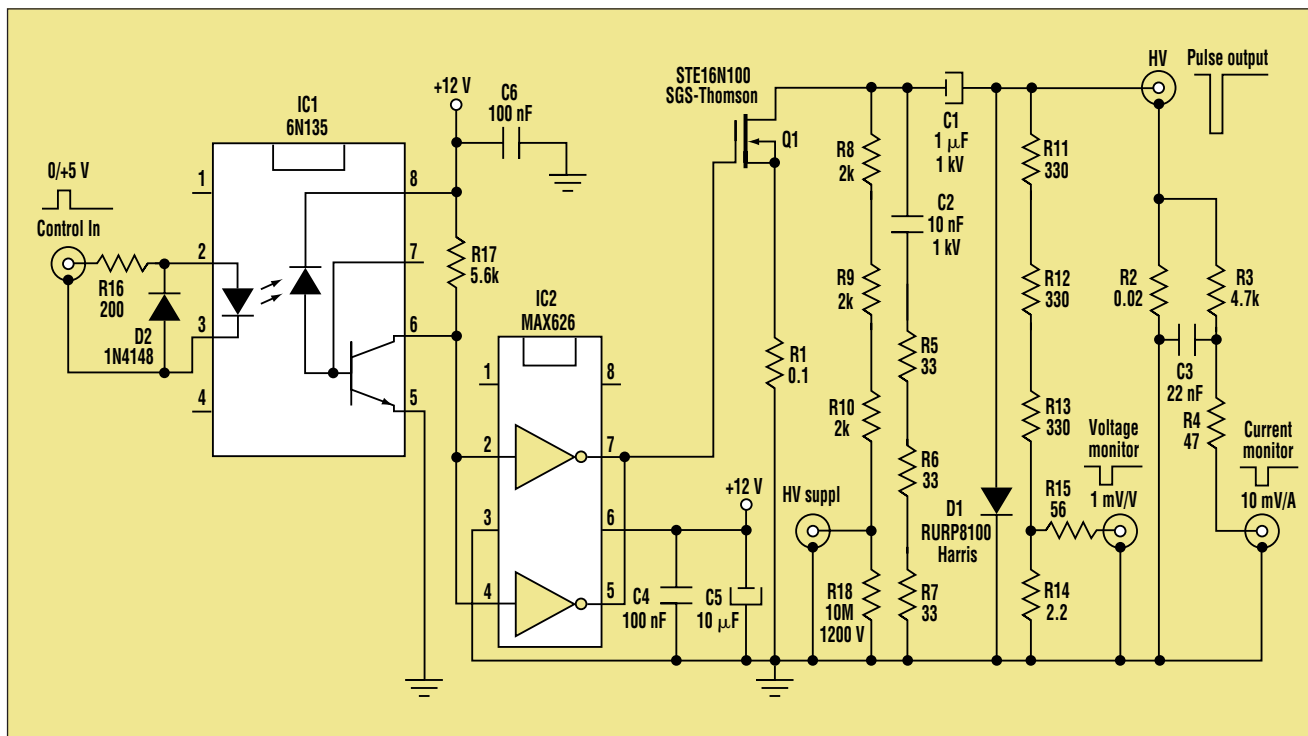
and D1 (see the figure). A 0-V control signal keeps the PowerFET Q1 in the off state. A 5-V signal on the control input operates the driver IC2, from which a 12-V signal is presented on the gate of the PowerFET Q1, bringing it into conduction. The output of the circuit becomes -HV volts as the negative terminal of C1 is now grounded. The pulse ends by making the control signal 0 V. Useful pulse length is limited by the voltage drop during the pulse (caused by discharging C1) and by the 100- $\mu$ s/64-A safe limit of the PowerFET. For the values shown, the circuit voltage drop is 10 V for a 1- $\mu$ s, 10-A pulse.

The short-circuit and overload protection is based on R1. When the output current is rising, the effective gate-source voltage of the PowerFET diminishes, enlarging the FET

resistance. With the given 0.1- $\Omega$  value, the output current is limited to 50 A. In a short-circuit situation, capacitor C1 can be fully (and safely) discharged in the PowerFET. Reverse voltages caused by inductive loads are eliminated by D1. When the circuit isn't operating, R14 discharges C1 for safety reasons.

Circuit layout is very important—a groundplane is needed to keep inductance low. C1 must be a low-inductance pulse capacitor. Even the FET driver IC2 needs a low-inductance layout and decoupling. During the leading-edge gate currents, up to 2 A are needed to charge the FET input capacitance. Resistors R1 and R2 have to be made of at least 10 paralleled discrettes to get a low series inductance. R4 and C3 compensate for the remaining inductance in R2 (the value of C3 can be changed for this). C2, R5, R6, and R7 form a snubber network to protect the FET against voltage spikes. The values for the voltage and current monitor levels are given for a 50- $\Omega$  load.

Higher currents can be obtained by duplicating the IC2-Q1-R1 stage and connecting them in parallel. R1 helps to equalize the current for each stage. A 100-A pulser has been successfully built in this manner.



Fast risetime pulses of 0 to 1000 V, with currents up to 50 A, can be generated by this simple, low-cost high-voltage power pulse circuit.