

Interconnect Impedance Measurements, Signal Integrity Modeling, Model Validation, and Failure Analysis

IConnect® TDR Software

TDA Systems, Inc.
www.tdasystems.com

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Outline

- **TDR Impedance Measurements in IConnect®**
- **Interconnect Signal Integrity Modeling and Model Validation in IConnect®**
- **Interconnect Failure Analysis in IConnect®**

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Collateral

- **Presentation Handouts**
www.tdasystems.com/training.htm
- **Application materials**
www.tdasystems.com/support.htm
- **TDR FAQ**
www.tdasystems.com/faq/faq.htm
- **TDR References**
www.tdasystems.com/bibliography.htm

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Signal Integrity Interconnect Significance

Signal Integrity (SI): Digital Becomes Analog

“At high frequencies ... crosstalk and signal reflections can be perceived as logic triggers, and can be responsible for erroneous signal patterns”

EE Times, April 17, 1998, Special Section on Interconnects

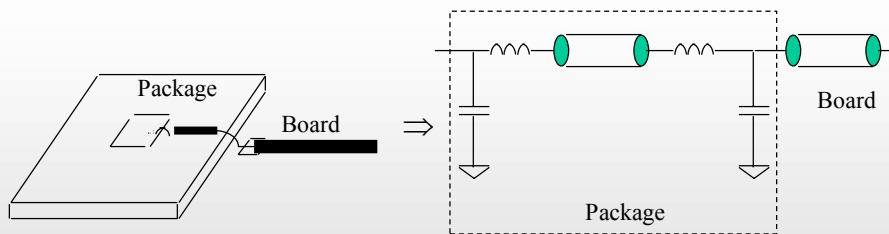
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Signal Integrity Interconnect Significance

Interconnects at High Speeds

- Interconnects become transmission lines
- Interconnect discontinuities become lumped L-C networks



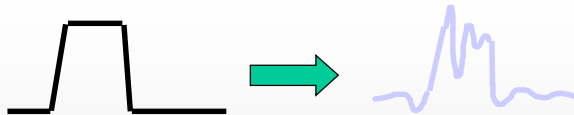
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Signal Integrity Interconnect Significance

Signal Integrity Issues

- Propagation delay
- Reflections
- Crosstalk
- Loss
- Ground bounce
- Dispersion



SPICE/IBIS simulations and *accurate interconnect models* are required

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Signal Integrity Interconnect Significance

Consequences of Poor Signal Integrity

- **Jitter and eye diagram degradation**
 - Result of losses and crosstalk
 - Model with lossy and coupled line models
- **Signal distortion, digital switching errors**
 - Result from crosstalk, reflections and ringing
 - Crosstalk -> need coupled line modeling
 - Reflections -> need impedance measurement accuracy and transmission line modeling
 - Ringing -> need lumped element and transmission line modeling

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Signal Integrity Interconnect Significance

Benefits of Addressing the Signal Integrity Early

- **Avoid recalls and design failures** \$
- **Get product to market in time** \$
 - Avoid delays in time-critical design phases
- **Lower design costs** \$
 - No redesigns results in savings!
- **Achieve higher-performance system** \$
 - Gain market share with a better product

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Signal Integrity Interconnect Significance

Critical Interconnect Components

- **PCB traces**
 - Single-run
 - Differential
 - On different layers
- **PCB Vias**
- **Connectors and cable-connector assemblies**
- **Packages and multichip modules**
- **Sockets**

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Failure Analysis Interconnect Significance

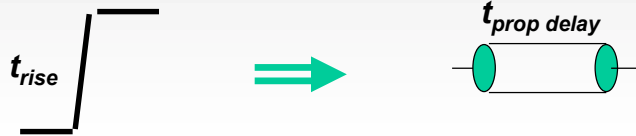
Failure Analysis Issues

- **Broken trace / bondwire (open)**
- **Lead to ground short**
- **Partial short or open**
- **Lead to lead short**
- **Plane to plane short**

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When is Interconnect Lumped?



Practical rule of “short” or “lumped” (RLC) interconnect

$$t_{rise} > t_{prop\ delay} \cdot 6$$

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What are you trying to learn today?

- TDR Measurement s → ✓
 - Measurement Basics
 - Impedance Measurements
 - Interconnect Probing and Fixturing
- Interconnect SI Modeling → ✓
 - IConnect® Modeling Methodology
 - L and C Computation
 - Transmission Line Modeling
 - Coupled and Differential Line Modeling
 - Lossy Line Modeling
- Interconnect FA → ✓
 - Open fault location
 - Short fault location

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Outline

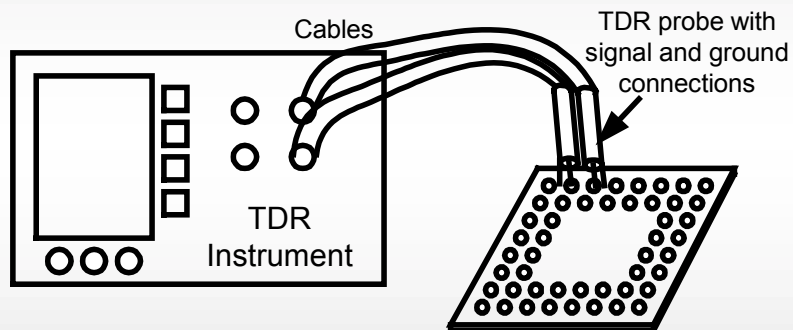
- TDR Impedance Measurements in IConnect®
 - Basics
 - True Impedance Profile
 - Probing and Fixturing
 - Interconnect Signal Integrity Modeling and Model Validation in IConnect®
 - Interconnect Failure Analysis in IConnect®

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TDR Measurements Basics

TDR Measurement Setup

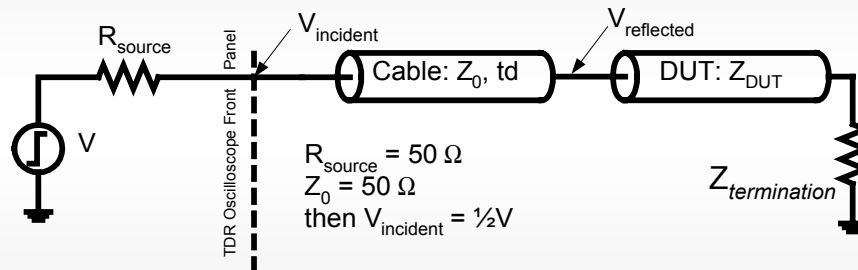


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TDR Measurements Basics

TDR Block Diagram

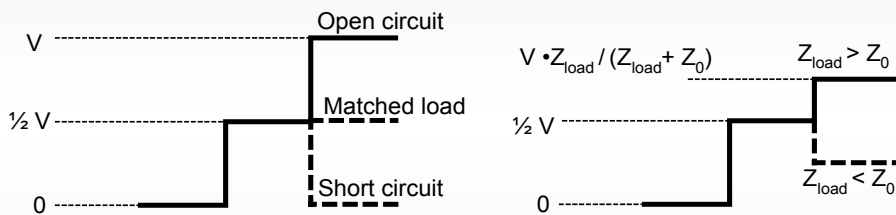


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TDR Measurements Basics

TDR Visual Representation



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TDR Measurements Basics

Practical Session

- Time base setup
- Vertical scale setup
- TDR setup
- Averaging and filtering
- Basic instrument calibration and operating conditions
- Normalization

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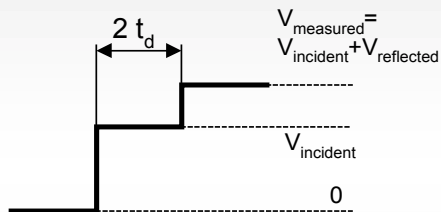


TDR Measurements Basics

TDR Basic Equations

$$\rho = \frac{V_{reflected}}{V_{incident}} = \frac{Z_{load} - Z_0}{Z_{load} + Z_0}$$

$$V_{reflected} = V_{incident} \cdot \frac{Z_{DUT} - Z_0}{Z_{DUT} + Z_0}$$



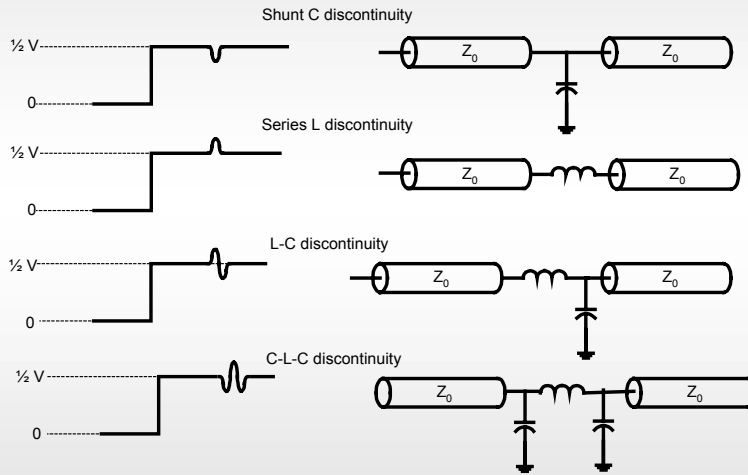
$$Z_{DUT} = Z_0 \cdot \frac{1 + \rho}{1 - \rho} = Z_0 \cdot \frac{V_{incident} + V_{reflected}}{V_{incident} - V_{reflected}} = Z_0 \cdot \frac{V_{measured}}{2 \cdot V_{incident} - V_{measured}}$$

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TDR Measurements Basics

Inductance and Capacitance Analysis



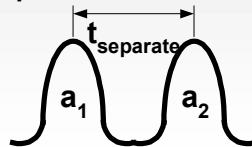
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TDR Measurements Basics

TDR Rise Time and Resolution

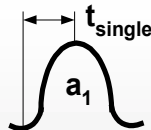
- Accepted rule of thumb for resolving two discontinuities



To resolve a_1 and a_2 as separate discontinuities:

$$t_{\text{separate}} > t_{\text{TDR_risetime}} / 2$$

- More real case: resolving a single discontinuity



a_1 is not resolved if

$$t_{\text{single}} \ll t_{\text{TDR_risetime}}$$

- Going beyond the TDR resolution and risetime: relative techniques
 - Signal integrity modeling – JEDEC standard
 - Failure analysis – golden device comparisons

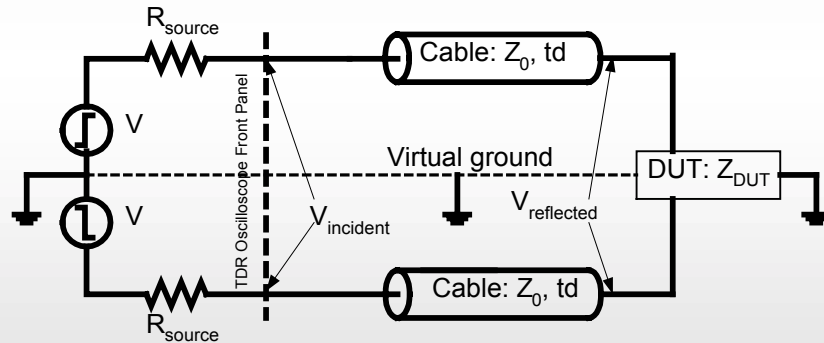
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TDR Measurements Basics

Differential TDR

- Virtual ground plane
- Even and odd mode measurements



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TDR Measurements Basics

Practical Session

- Time base setup
- Vertical scale setup
- TDR setup
- Averaging and filtering
- Basic instrument calibration and operating conditions

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Outline

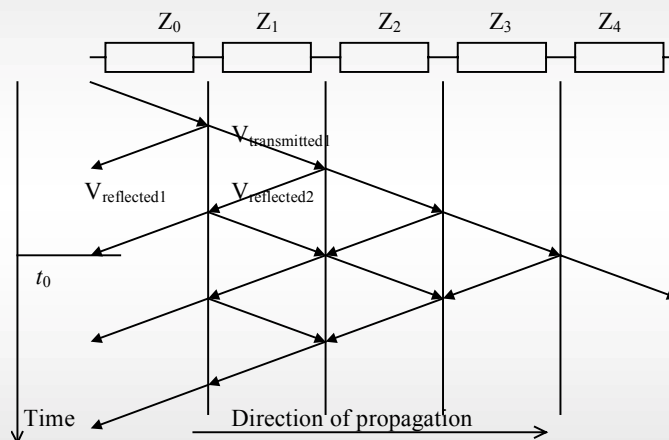
- TDR Impedance Measurements in IConnect®
 - Impedance Measurements and IConnect® TDR Software True Impedance Profile
Appnote: "PCB Interconnect Characterization from TDR Measurements"
 - Probing and Fixturing
- Interconnect Signal Integrity Modeling and Model Validation in IConnect®
- Interconnect Failure Analysis in IConnect®

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Impedance Accuracy

TDR Multiple Reflection Effects



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Impedance Accuracy

IConnect Computation of the True Impedance Profile

$$V_{reflected\ 1} = \rho_1 V_{incident\ 1}$$

$$V_{reflected\ 2} = t_1^2 \rho_2 V_{incident\ 1} + \rho_1 V_{incident\ 2}$$

$$V_{reflected\ 3} = (t_1^2 t_2^2 \rho_{32} - t_1^2 \rho_2^2 \rho_1) V_{incident\ 1} + t_1^2 \rho_2 V_{incident\ 2} + \rho_1 V_{incident\ 3}$$

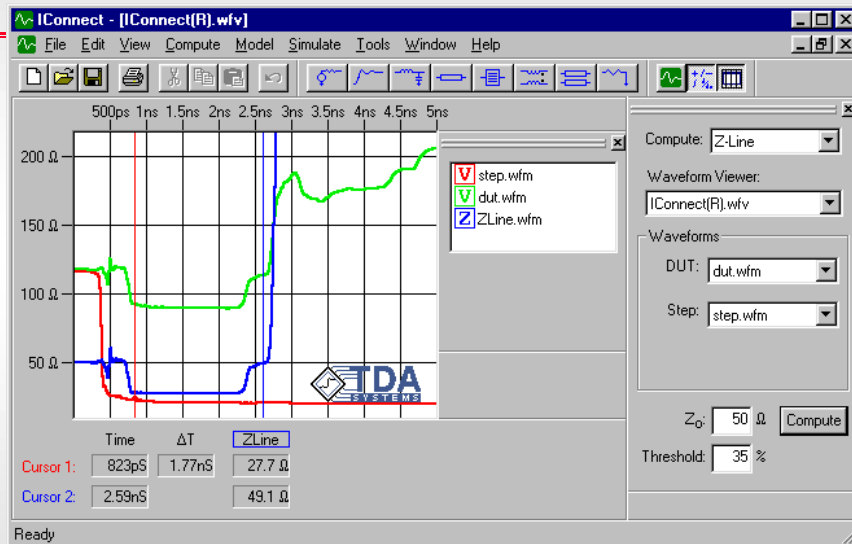
$$\begin{bmatrix} V_{reflected1} \\ V_{reflected2} \\ V_{reflected3} \\ \vdots \\ V_{reflectedn} \end{bmatrix} = \begin{bmatrix} k_1 & 0 & 0 & \cdots & 0 \\ k_2 & k_1 & 0 & 0 & 0 \\ k_3 & k_2 & k_1 & 0 & \vdots \\ \vdots & \vdots & \vdots & \ddots & 0 \\ k_n & k_{n-1} & k_{n-2} & \cdots & k_1 \end{bmatrix} \begin{bmatrix} V_{incident1} \\ V_{incident2} \\ V_{incident3} \\ \vdots \\ V_{incidentn} \end{bmatrix}$$

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Impedance Accuracy

Board Trace IConnect® Z-line

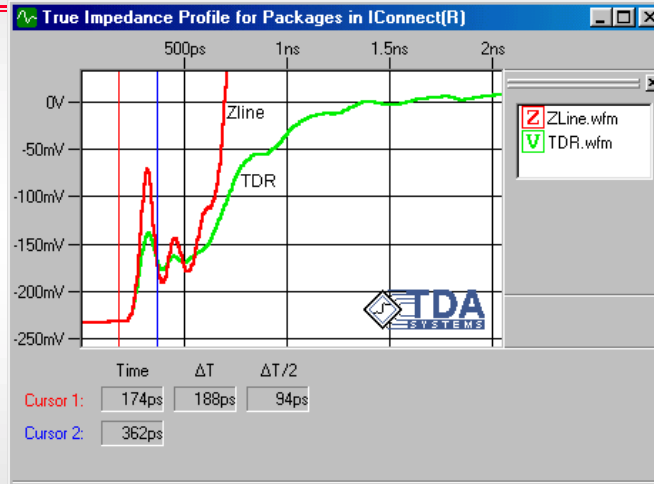


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Impedance Accuracy

Package Trace IConnect® Z-line



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Impedance Accuracy

IConnect® TDR Software Z-line Algorithm

- Ensures accurate impedance measurements
- Also called Impedance De-embedding, Peeling, Inverse Scattering
- Minimizes effects of multiple reflections
- Computes true impedance profile
- Enables model generation
 - compute SPICE model output
 - cursor readout for Z, td, L and C
- **Limitations:**
 - data noise may interfere with accuracy
 - use scope averaging
 - use software noise filtering
 - line loss may cause problems

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Outline

- TDR Impedance Measurements in IConnect®
 - Interconnect Probing and Fixturing
 - *Quick Guide: “Interconnect Probing Quick Guide”*
- Interconnect Signal Integrity Modeling and Model Validation in IConnect®
- Interconnect Failure Analysis in IConnect®

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Probing and Fixturing

Probing and Fixturing Issues

- ***Probing is the weakest link!***
- **Start with a probe**
 - 50 Ohm for TDR measurements
 - must be rugged and inexpensive
 - ensure stable repeatable contact
 - large pitch* means small bandwidth
 - variable pitch means poor repeatability
 - ensure sufficient compliance



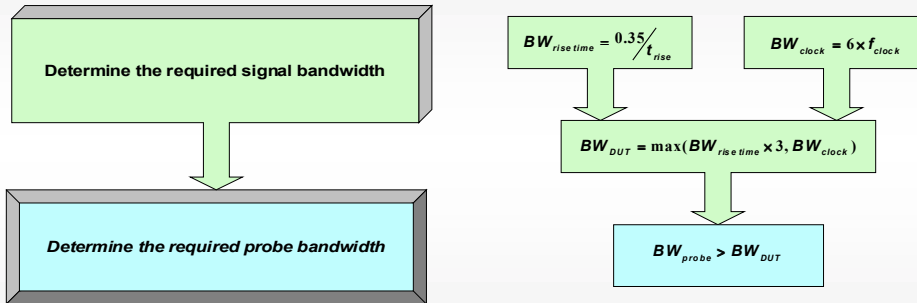
* Pitch: center-to-center signal to ground pad spacing

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Probing and Fixturing

Probe Bandwidth Selection



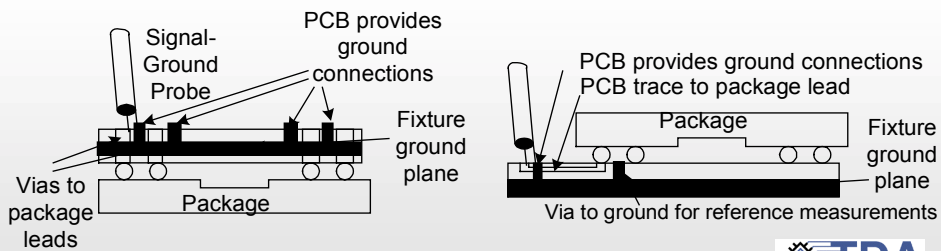
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Probing and Fixturing

Package and Connector Probing

- Use a high-quality probe (and positioner)
- Need an interface adapter or fixture to probe
- Fixturing requirements
 - Reproduce the real application environment
 - Ensure easy fixture de-embedding (reference short and open structures may be needed)



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Board Probing

- Ensure good contact to a via (via probing is a challenge for microwave probe)
- Ensure ground contacts near your signals
- Variable pitch is a *sad* necessity if there are no ground nearby
 - TDR probes from TDR manufacturer
 - Variable pitch probes from probe manufacturers
 - Measurements suffer from poor repeatability and decrease the instrument usable bandwidth

Probing vs. Fixturing

Probing advantages:

- Maximum flexibility for multiple device measurements
- No fixture de-embedding required

But:

- Requires DUT to have easily accessible contact areas
- Positioning system may be expensive

Fixturing advantages:

- Evaluate the DUT in its intended environment of use (example: package on a board)
- Great flexibility for *specific* DUT

But:

- Difficult to change after the fixture has been designed
- Must de-embed fixturing from measurements

👉 These approaches are complementary!

👉 Fixturing is thinking ahead about how you will probe!

Outline

- ✓ TDR Impedance Measurements in IConnect®
- Interconnect Signal Integrity Modeling in IConnect®
 - IConnect® TDR Software Modeling Methodology
 - L and C Computation and Short Interconnect Analysis
 - Single-ended TDR Transmission Line Modeling
 - Differential TDR Coupled-Transmission Line Modeling
 - Lossy Transmission Line Modeling
- Interconnect Failure Analysis in IConnect®

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IConnect Modeling Methodology

Goals and Model Validity

- Goal: create SPICE /IBIS models to predict interconnect performance
- Model *required range of validity* is defined by a greater of
 - signal rise time: $f_{bw} = 0.35 / t_{rise}$
- It may be desired to extend the required range of model validity beyond f_{bw}

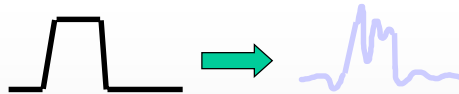
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IConnect Modeling Methodology

How Will the Results Be Used?

- Simulate your I/O Bus from Driver to Receiver
 - In SPICE or IBIS
- Predict signal integrity issues
 - Jitter, loss, crosstalk, reflections, ringing



- Optimize the Interconnect for best signal integrity



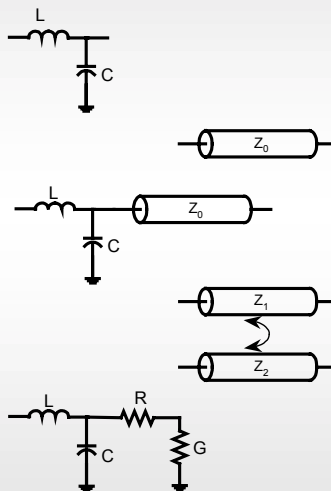
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IConnect Modeling Methodology

Interconnect Models

- Lumped
- Distributed
- Mixed
- Coupled
- Lossy



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IConnect Modeling Methodology

Why Measurement-Based Modeling?

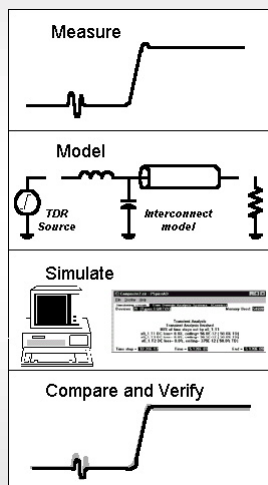
- Analytical model may differ from reality:
 - Accuracy and assumptions of the analytical tool
 - Material properties may not be available
 - Geometries may not be available
 - Component manufacturing tolerances
- Accurate measurement is the true representation of reality
- Analytical models must be *validated with measurement*
- Accurate models achieved through prototype characterization

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IConnect Modeling Methodology

Measurement Based Approach



- TDR Measurements
- Extracted interconnect, TDR source model
- Direct link to simulators
- Automatic comparison of simulation and measurement in IConnect waveform viewer

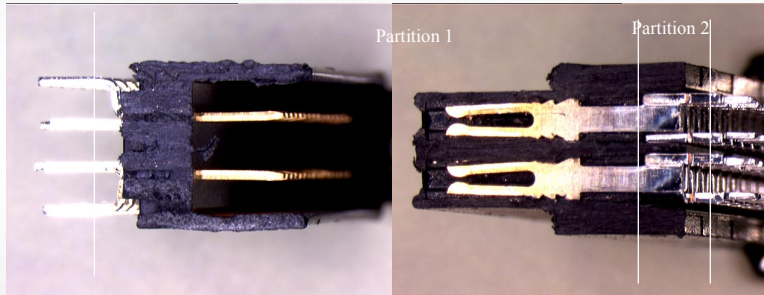
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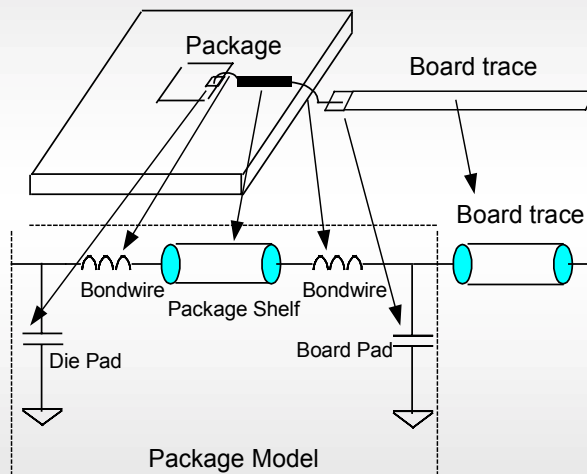
Connector: Correlate Model to Physical Structure

PCB section

Cable section

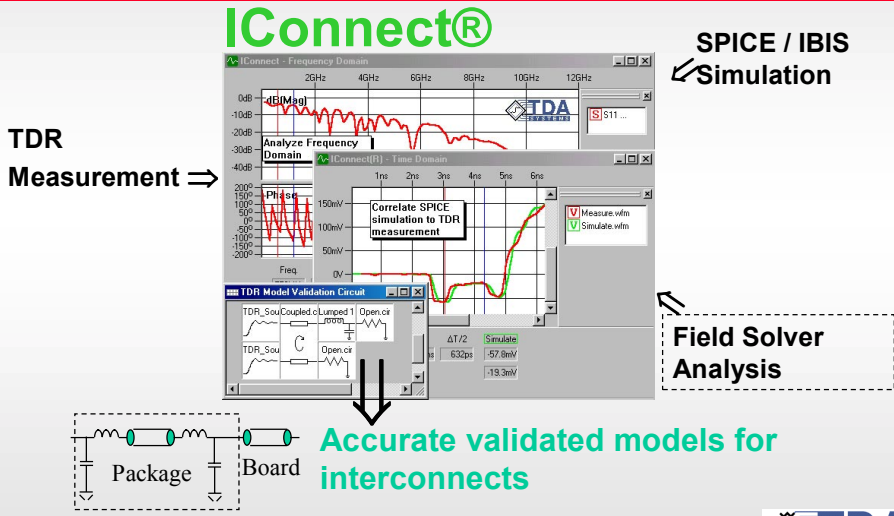


Package: Correlate Model to Physical Structure



IConnect Modeling Methodology

IConnect® TDR Software



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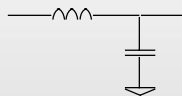


IConnect Modeling Methodology

Frequency or Time Domain?

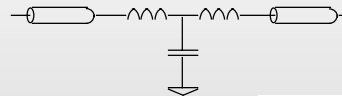
VNA:

- Steady state measurements
- Very high dynamic range
- “Black box” S-parameter results
- Single-element modeling capabilities



TDR:

- Transient measurements
- Windowing capability
- Can model complex structures
 - but – multiple reflections impede accuracy



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IConnect Modeling Methodology

Frequency or Time Domain

- **Interconnect properties**
 - Typically are complex multi-element structures
 - Interconnects are broadband structures
 - Measurements do not require high dynamic range
 - Interconnects are *NOT* strongly resonant structures, 40dB dynamic range is sufficient
 - Measurement **DO** require good spatial (time) resolution that TDR provides
- **Summary:**
 - Use Time Domain as primary modeling tool
 - Use frequency domain to model secondary effects

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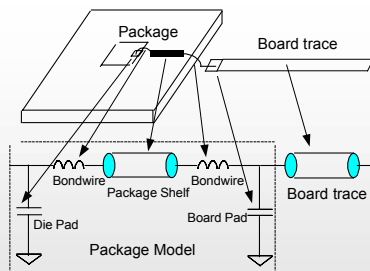


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Behavioral or Physical Model?

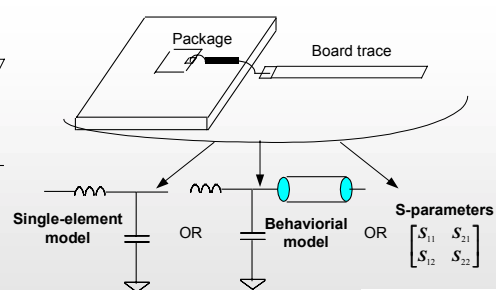
- **Physical (TDR)**
 - Correlates to the interconnect geometry
 - Allows to isolate the signal integrity issues
- **Behavioral (VNA)**
 - Does not correlate to geometry
 - Matches the frequency or time response

TDR interconnect modeling



Physical model: correlates to the DUT geometry

VNA interconnect modeling



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SPICE or IBIS?

- **Interconnect models are not substantially different in SPICE and IBIS**
 - You can create either models with TDR
- **Main functional difference is in active component models (driver/receiver)**
- **You choice which to use for simulations**

Outline

- ✓ **TDR Impedance Measurements in IConnect®**
- **Interconnect Signal Integrity Modeling in IConnect®**
 - **L and C Computation and Short Interconnect Analysis**
Appnote: "TDR Techniques for Characterization and Modeling of Electronic Packaging"
 - **Single-ended TDR Transmission Line Modeling**
 - **Differential TDR Coupled-Transmission Line Modeling**
 - **Lossy Transmission Line Modeling**
- **Interconnect Failure Analysis in IConnect®**

ICConnect Short Interconnect Modeling

Using a Lumped Model for an Interconnect



Practical rule of “short” or “lumped” (RLC) interconnect

$$t_{rise} > t_{prop\ delay} \cdot 6$$

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ICConnect Short Interconnect Modeling

What Are Short Interconnects?

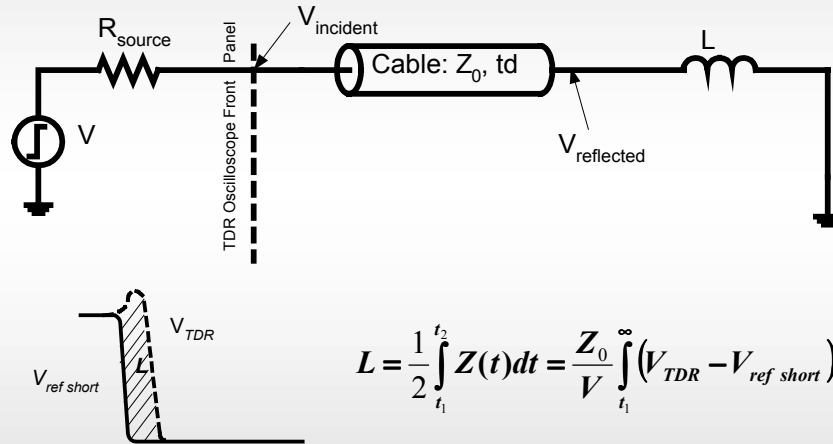
- Example: at 500ps rise time, the following interconnects can be considered short:
 - IC packages
 - Connectors
 - Sockets
 - Vias on the board

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IConnect Short Interconnect Modeling

Single Parasitic Inductance

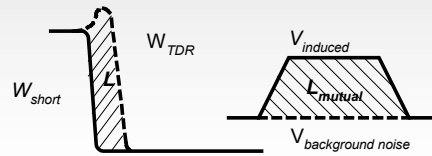
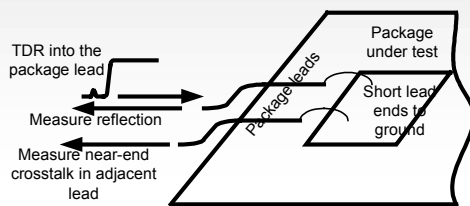


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IConnect Short Interconnect Modeling

Single-Ended TDR: Package Lead Inductance L Measurements



$$L_{self} = \frac{Z_0}{2 \cdot V} \cdot \int_0^{\infty} (W_{TDR} - W_{short}) dt$$

$$L_{mutual} = \frac{Z_0}{2 \cdot V} \cdot \int_0^{\infty} (W_{induced} - W_{background}) dt$$

- **TDR waveform:**
 - TDR into package lead.
 - Short all the leads to ground on the inside of the package.
 - Short the leads that are not being measured to ground on the outside of the package.
- **Short waveform:**
 - TDR into the "short"; connect the probe signal contact to ground on a conductive (metal) pad

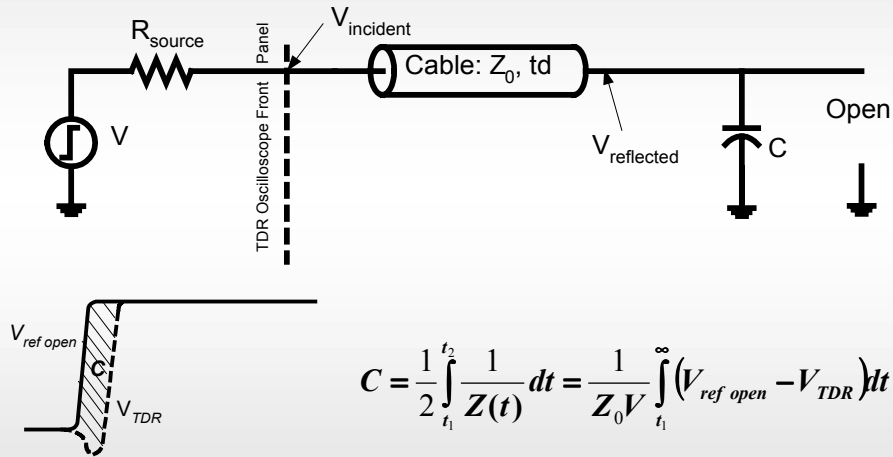
- **Induced waveform:**
 - Measure near end crosstalk with far end of the victim open-ended
- **Background waveform:**
 - Corrects for the noise and scope DC offset

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ICConnect Short Interconnect Modeling

Single Parasitic Capacitance

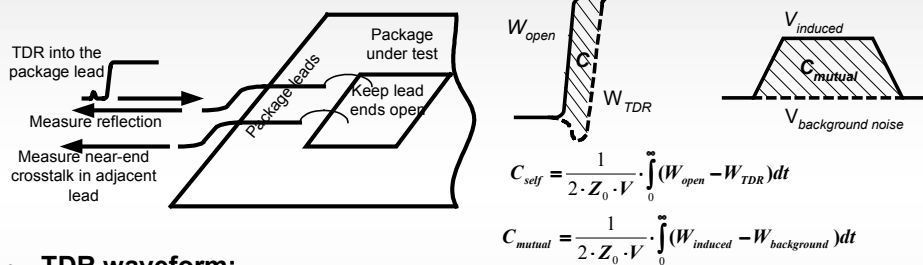


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Single-Ended TDR: Package Lead Capacitance C Measurements



- **TDR waveform:**

- **TDR into package lead**
- Short the leads that are not being measured to ground on the outside of the package

- **Open waveform:**

- TDR into the "open"; disconnect the probe from the DUT or remove the DUT from the fixture

- **Induced waveform:**

- Measure near end crosstalk with far end of the victim open-ended

- **Background waveform:**

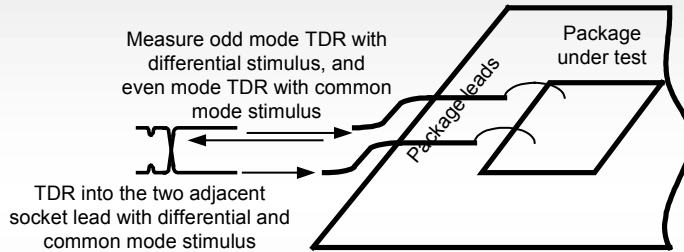
- Corrects for the noise and scope DC offset

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IConnect Short Interconnect Modeling

Even-Odd Mode Impedance Profile



$$L_{self} = \frac{1}{2} (Z_{even} t_{even} + Z_{odd} t_{odd})$$

$$C_{tot} = \frac{1}{2} \left(\frac{t_{odd}}{Z_{odd}} + \frac{t_{even}}{Z_{even}} \right)$$

$$L_m = \frac{1}{2} (Z_{even} t_{even} - Z_{odd} t_{odd})$$

$$C_m = \frac{1}{2} \left(\frac{t_{odd}}{Z_{odd}} - \frac{t_{even}}{Z_{even}} \right)$$

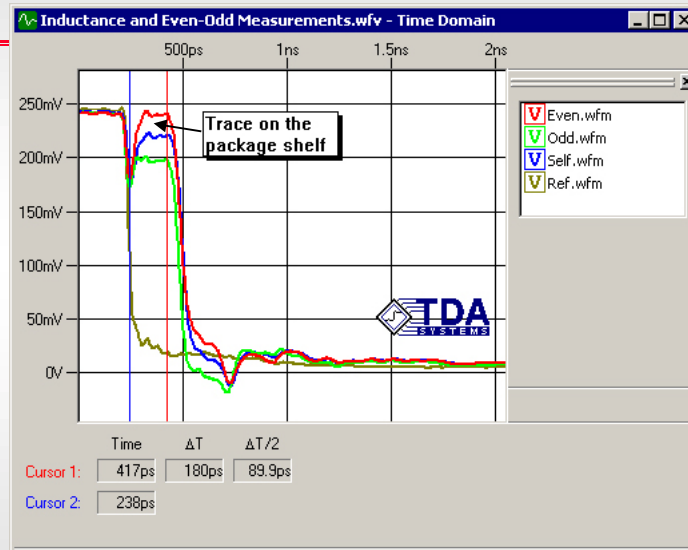
$$C_{total} = C_{self} + C_m$$

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IConnect Short Interconnect Modeling

Inductance and Even-Odd Mode Measurements

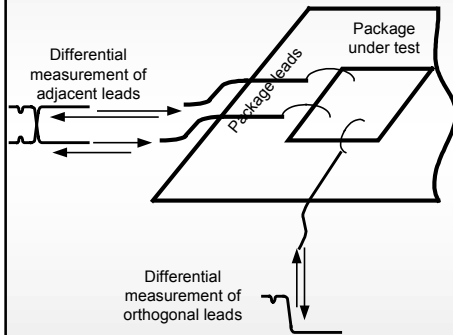


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IConnect Short Interconnect Modeling

Adjacent-Opposite Mode Analysis



$$L_{\text{total adjacent}} = L_{\text{self}} - L_{\text{mutual}}$$

$$L_{\text{self}} = L_{\text{total opposite}}$$

$$L_{\text{mutual}} = L_{\text{total opposite}} - L_{\text{total adjacent}}$$

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IConnect Short Interconnect Modeling

Techniques for Various Packages

	Model required	Primary modeling method	Secondary modeling method
SOIC	C	Lumped	Lumped
	L	Adjacent-opposite	Lumped
TSOP	C	Lumped	Lumped
	L	Adjacent-opposite	Lumped
PGA	Distributed, coupled	Impedance profile	Even-odd impedance
QFP	Distributed-coupled	Even-odd impedance	Lumped, adjacent-opp.
Small BGA, LGA	Distributed-coupled	Even-odd impedance	Lumped, adjacent-opp.
Large BGA, LGA	Distributed-coupled	Impedance profile	Even-odd impedance
MCM	Distributed-coupled	Impedance profile	Even-odd impedance
CSP	C	Lumped	Lumped
	L	Adjacent-opposite	Lumped

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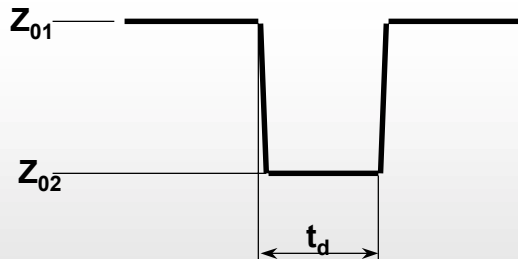
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IConnect Single-Ended TDR Techniques

Transmission line Z and t_d

- Directly available from impedance profile
- Eliminate confusion about:
 - exact impedance value
 - exact electrical length of the lines



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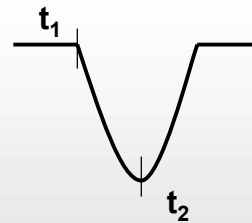
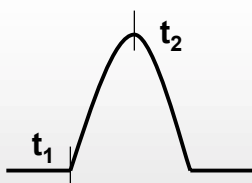


ICConnect Single-Ended TDR Techniques

Via L and C

$$L = \frac{1}{2} \int_{t_1}^{t_2} Z(t) dt$$

$$C = \frac{1}{2} \int_{t_1}^{t_2} \frac{1}{Z(t)} dt$$

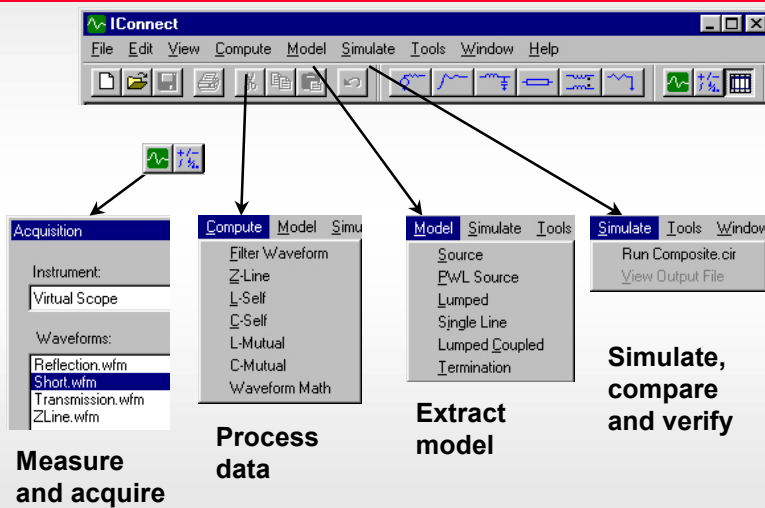


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ICConnect Single-Ended TDR Techniques

ICConnect® Modeling Process



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IConnect Single-Ended TDR Techniques

Modeling in IConnect TDR Software

The screenshot displays the IConnect software interface. On the left, a TDR plot shows impedance versus time. The y-axis ranges from 20 to 140 Ω , and the x-axis ranges from 500ps to 3ns. A red curve shows the impedance response, with a step change around 1.84ns. A blue vertical bar highlights a region between 2.5ns and 3ns. Below the plot, cursor data is shown:

Cursor	Time	ΔT	ZLine
Cursor 1	795ps	1.84ns	27.8 Ω
Cursor 2	2.63ns		49.3 Ω

On the right, a green box contains the following circuit model text:

```
* Name: Automatically Generated
.subckt Single port1 port2 gnd_
***** Partition #1
c1 port1 gnd_ 456f
l1 port1 1 1.05n
***** Partition #2
t1 1 gnd_ 2 gnd_ Z0=50.8 TD=125p
.....
***** Partition #4
t3 3 gnd_ port2 gnd_ Z0=48.2
TD=190p
.ends
```

The bottom right corner features the logo for The Interconnect Modeling Company™ and TDA SYSTEMS.

IConnect Single-Ended TDR Techniques

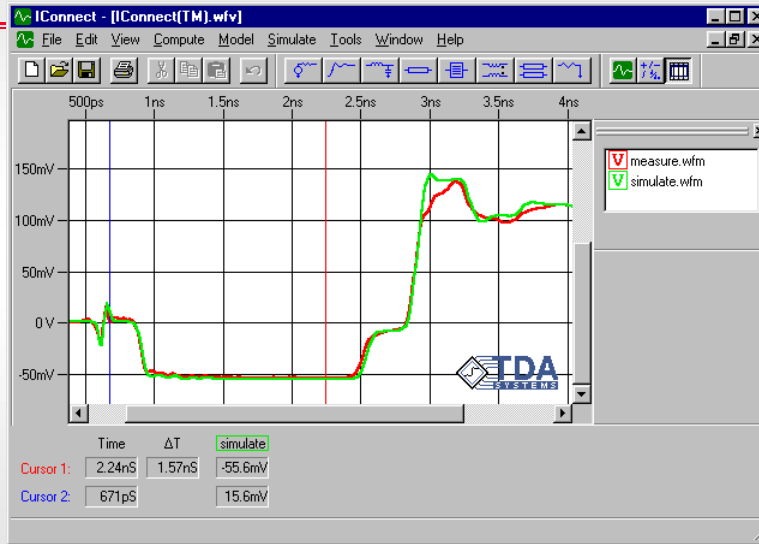
Prepare to Simulate and Validate

The screenshot shows the IConnect software interface with multiple windows. The main window displays a TDR plot similar to the one in the first slide. A 'Composite.cir' window shows a circuit diagram with components labeled 'PWL.cir', 'Single.cir', and 'Open.cir'. A 'Pwr' window shows a power waveform plot. A 'Partitions' dialog box is open, showing settings for Z₀ (49.5 Ω) and ΔT (183ps). A '100k Ω ' component is shown in a separate window.

The bottom right corner features the logo for The Interconnect Modeling Company™ and TDA SYSTEMS.

IConnect Single-Ended TDR Techniques

Simulation and Validation Results

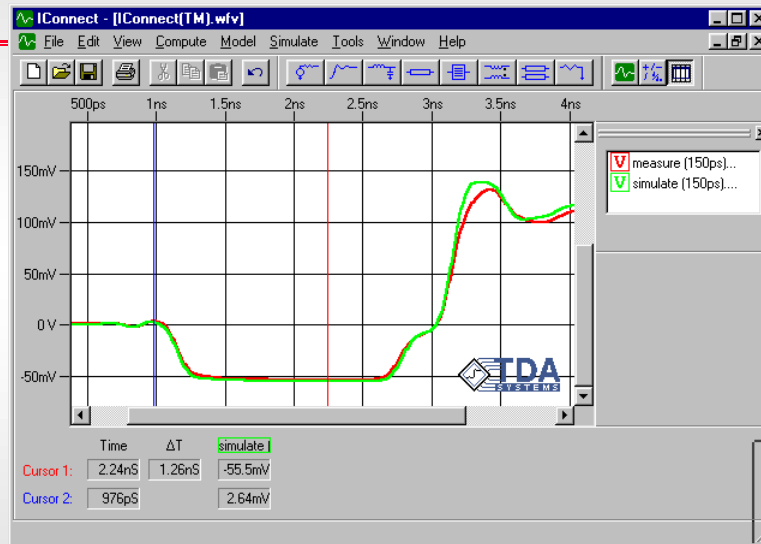


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IConnect Single-Ended TDR Techniques

Using Rise Time Filtering to Achieve Simple Models



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Outline

- ✓ TDR Impedance Measurements in IConnect®
- Interconnect Signal Integrity Modeling in IConnect®
 - Differential TDR Coupled Line Modeling
Appnote: "Characterization of Differential Interconnect from TDR Measurements"
 - Lossy Transmission Line Modeling
- Interconnect Failure Analysis in IConnect®

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IConnect Differential TDR Techniques

Coupled Line Models Predict:

- Differential line signal propagation
- Single ended and differential crosstalk
 - Forward
 - Backward
 - Re-reflection
- Crosstalk-induced jitter

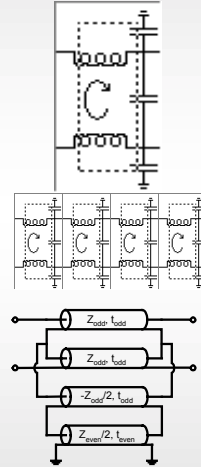
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IConnect Differential TDR Techniques

Differential Line Modeling

- **Short interconnect**
 - use lumped-coupled model
- **Long interconnect**
 - split lines in multiple segments
- **Longer yet interconnect**
 - symmetric distributed coupled line model

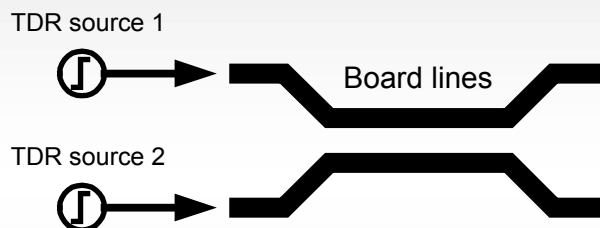


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IConnect Differential TDR Techniques

Symmetrical Coupled Line Model



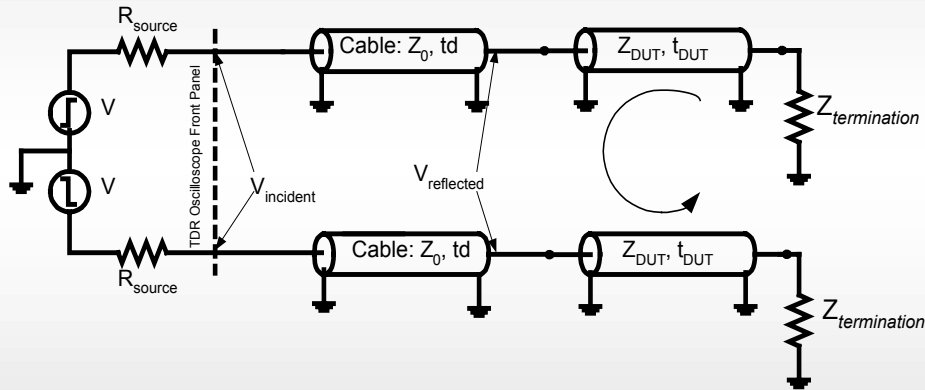
- **Assumptions:**
 - the lines are symmetrical
 - TDR pulses are symmetrical
 - TDR pulses arrive at the lines at the same time at the beginning of both lines

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ICnect Differential TDR Techniques

Differential TDR Measurement Setup



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ICnect Differential TDR Techniques

Even/Odd vs. Common/Differential

$$Z_{odd} = \sqrt{\frac{L_{self} - L_m}{C_{tot} + C_m}}$$

$$Z_{even} = \sqrt{\frac{L_{self} + L_m}{C_{tot} - C_m}}$$

$$t_{odd} = l\sqrt{(L_{self} - L_m)(C_{tot} + C_m)} \quad t_{even} = l\sqrt{(L_{self} + L_m)(C_{tot} - C_m)}$$

$$Z_{differential} = 2 \cdot Z_{odd}$$

$$Z_{common} = Z_{even} / 2$$

$$t_{differential} = t_{odd}$$

$$t_{common} = t_{even}$$

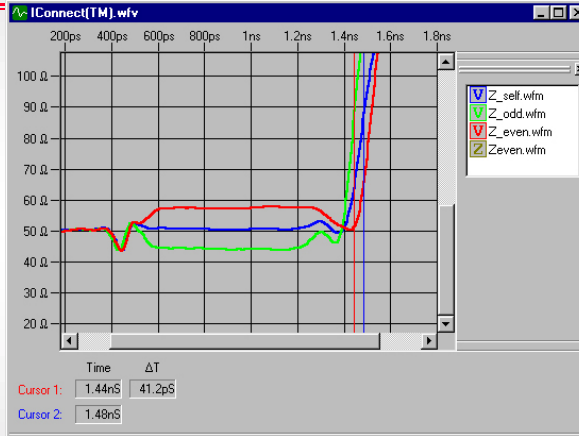
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IConnect Differential TDR Techniques

Even and Odd Impedance Profile Example

- $Z_{\text{even}} > Z_{\text{self}} > Z_{\text{odd}}$
- $t_{\text{even}} > t_{\text{self}} > t_{\text{odd}}$



- **Note:**
 - odd mode = differential measurement (two TDR sources of opposite polarity)
 - even mode = common mode measurement (two TDR sources of the same polarity)

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IConnect Differential TDR Techniques

L-C Even-Odd Mode Analysis for Line with Constant Impedance

$$L = \frac{1}{2}(t_{\text{even}} Z_{\text{even}} + t_{\text{odd}} Z_{\text{odd}})$$

$$C = \frac{t_{\text{even}}}{Z_{\text{even}}}$$

$$L_m = \frac{1}{2}(t_{\text{even}} Z_{\text{even}} - t_{\text{odd}} Z_{\text{odd}})$$

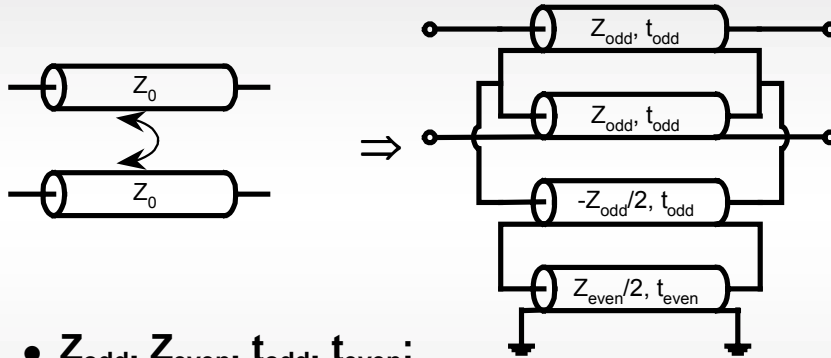
$$C_m = \frac{1}{2} \left(\frac{t_{\text{odd}}}{Z_{\text{odd}}} - \frac{t_{\text{even}}}{Z_{\text{even}}} \right)$$

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IConnect Differential TDR Techniques

IConnect Symmetrical Coupled Line Model



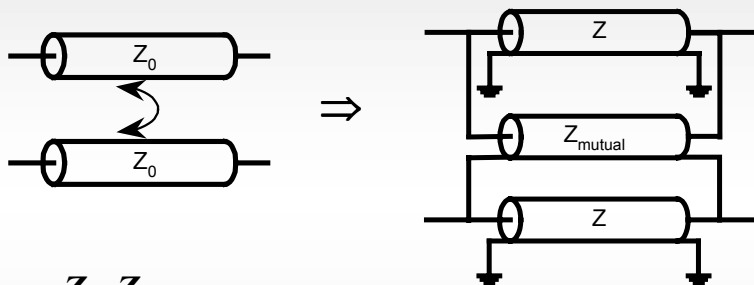
- Z_{odd} , Z_{even} , t_{odd} , t_{even} :
directly obtained from odd and even impedance profiles

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IConnect Differential TDR Techniques

IConnect Simplified Symmetrical Coupled Model



$$Z = Z_{even}$$

$$Z_m = \frac{2Z_{odd}Z_{even}}{Z_{even} - Z_{odd}}$$

Note: $Z_0 = \sqrt{Z_{odd}Z_{even}}$

! assume: $t_{odd} = t_{even}$!

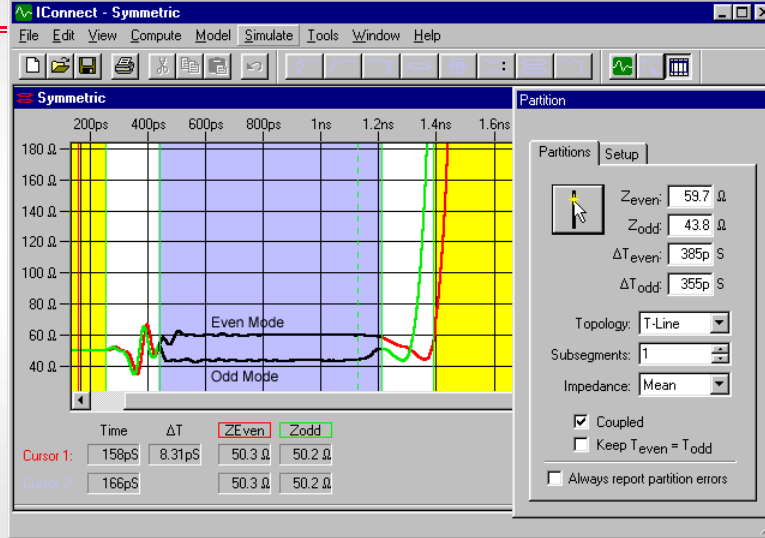
Alternatively, for differential lines: $t_{mutual} = t_{odd}$

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IConnect Differential TDR Techniques

IConnect Differential Line Modeling

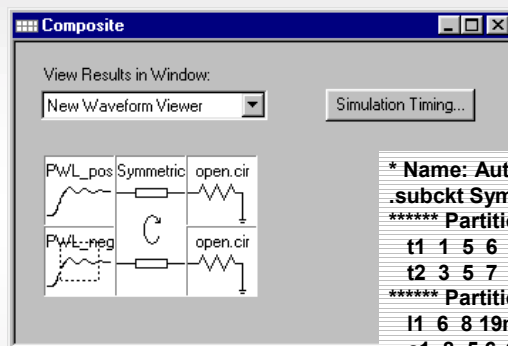


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IConnect Differential TDR Techniques

Composite Model Generation



```

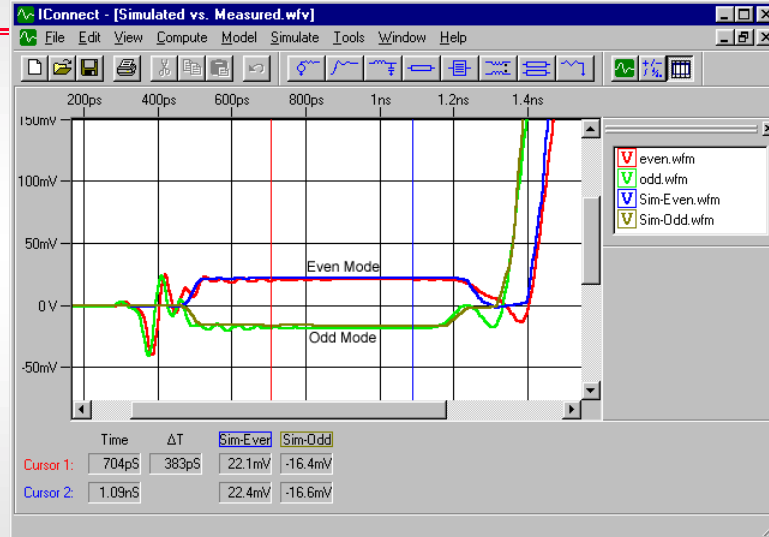
* Name: Automatically Generated
.subckt Symmetric 1 2 3 4 5
***** Partition #1
t1 1 5 6 5 Z0=49.7 TD=92.3p
t2 3 5 7 5 Z0=49.7 TD=92.3p
***** Partition #2
l1 6 8 19n
c1 8 5 6.44p
l2 7 9 19n
c2 9 5 6.44p
c3 8 9 716f
k1 l1 l2 207m
.ends
    
```

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IConnect Differential TDR Techniques

Model Validation in IConnect

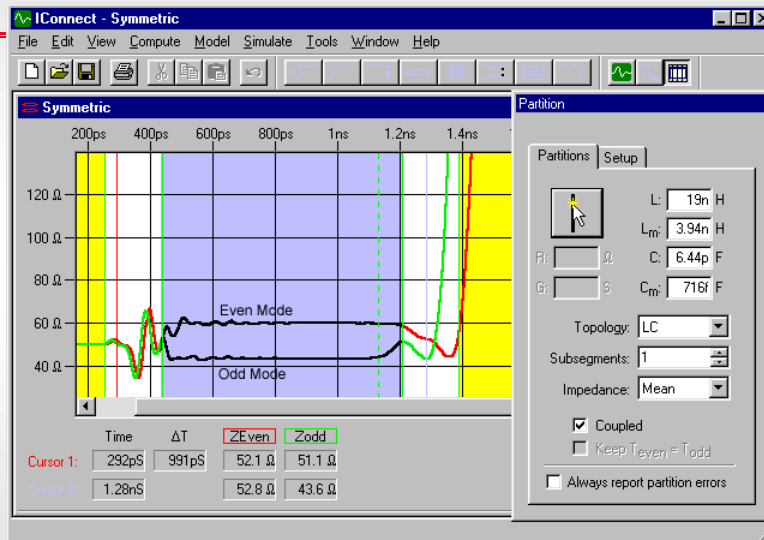


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IConnect Differential TDR Techniques

Coupled LC Computation in IConnect



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Outline

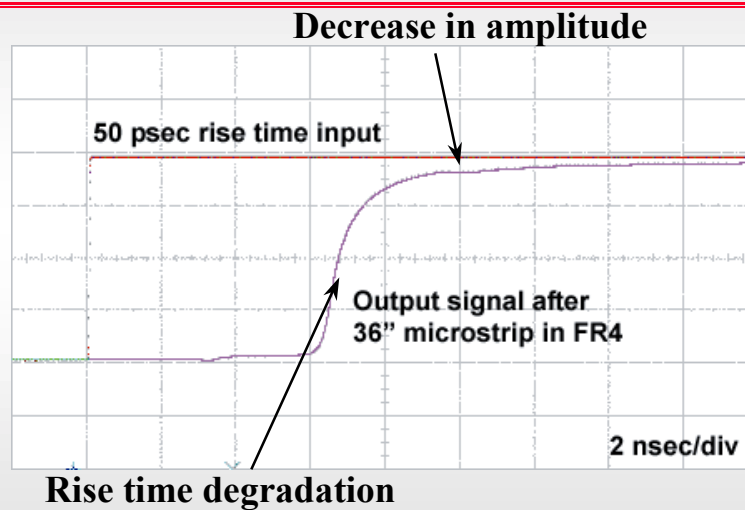
- ✓ TDR Impedance Measurements in IConnect®
- Interconnect Signal Integrity Modeling in IConnect®
 - TDT, Lossy Line Modeling and Eye Diagram
 - Appnote: "Practical Characterization of Lossy Transmission Lines Using TDR"*
 - Appnote: "Ensuring Signal Integrity... TDR and Frequency Domain Analysis Can Do the Trick"*
- Interconnect Failure Analysis in IConnect®

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TDT and IConnect Lossy Lines

Effect of Loss



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TDT and IConnect Lossy Lines

Rise time degradation



$$t_{interconnect} = \frac{0.35}{BW_{interconnect}}$$

$$t_{r final} = \sqrt{t_{r signal}^2 + t_{interconnect}^2}$$

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TDT and IConnect Lossy Lines

Lossy Line Modeling

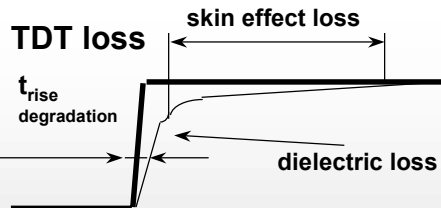
- DC resistive losses

TDR loss



- Skin effect losses

$$R_{skin} = R_0 + R_s \cdot \sqrt{f}$$



- Dielectric losses

$$G_{dielectric} = G_0 + G_d \cdot f$$

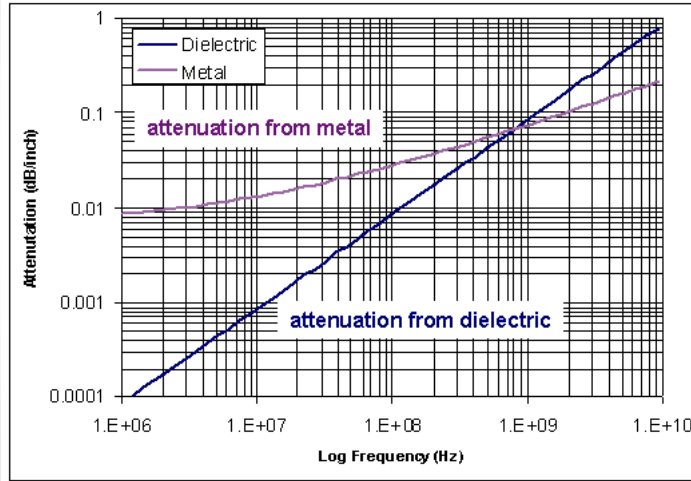
- Dispersion

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TDT and IConnect Lossy Lines

Skin Effect vs. Dielectric Loss



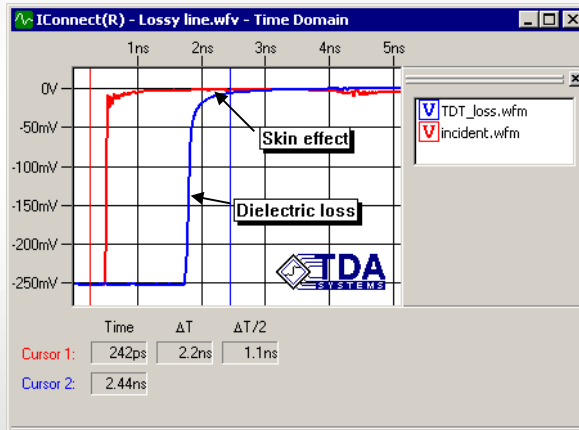
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TDT and IConnect Lossy Lines

IConnect Lossy Line Modeling

Use TDT to extract losses directly from time domain measurement

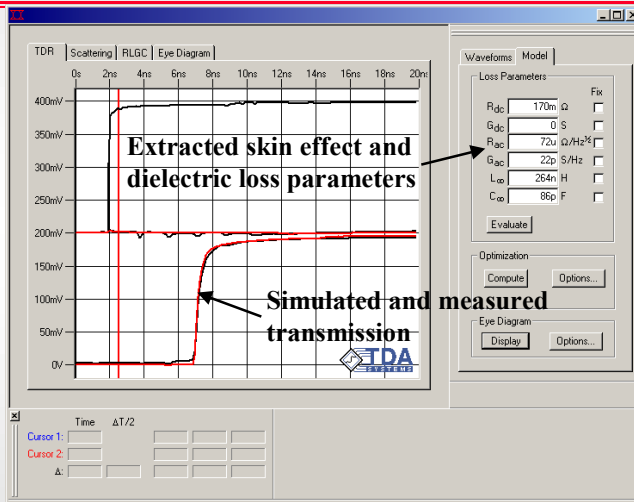


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TDT and IConnect Lossy Lines

Compute Skin Effect, Dielectric Loss, RLGC(F)

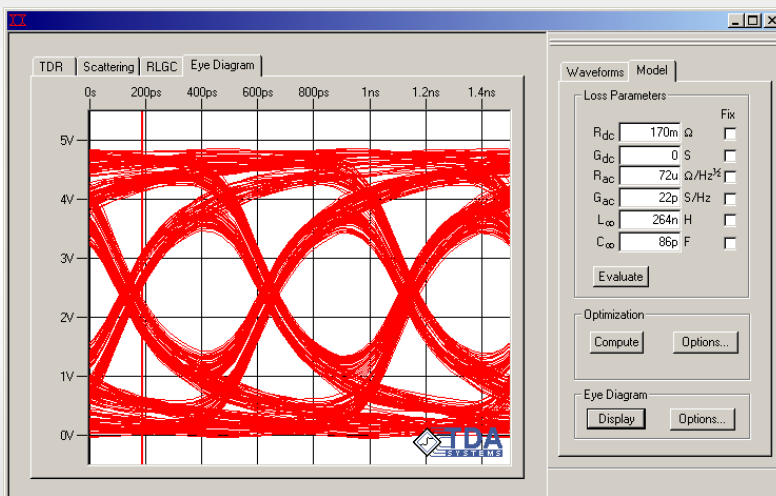


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TDT and IConnect Lossy Lines

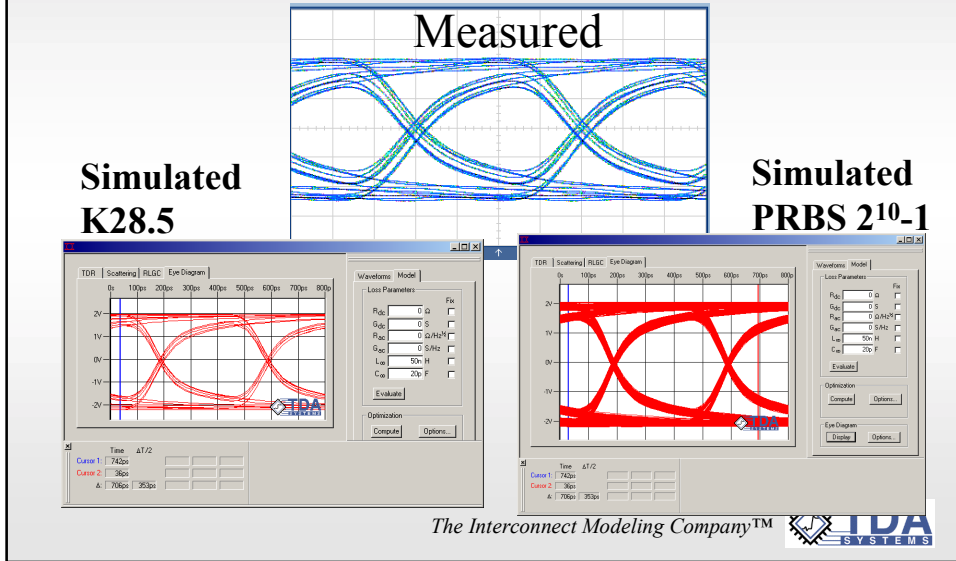
Loss-Based Eye Diagram Degradation



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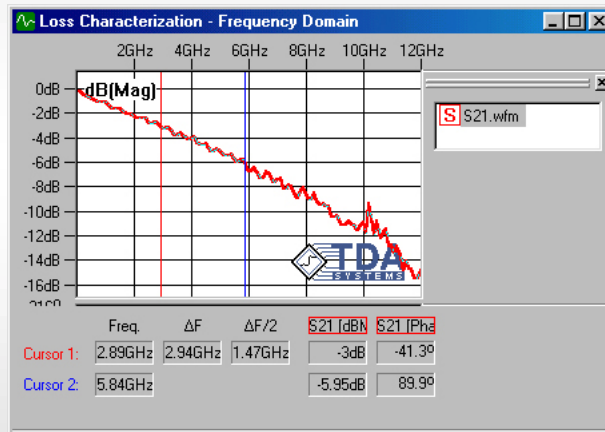
Predicted and Measured Eye Diagrams



TDT and IConnect Lossy Lines

Lossy Line Modeling

Measure TDT, compute S21 in IConnect



Outline

- ✓ TDR Impedance Measurements in IConnect®
- Interconnect Failure Analysis in IConnect®
- Interconnect Signal Integrity Modeling in IConnect®

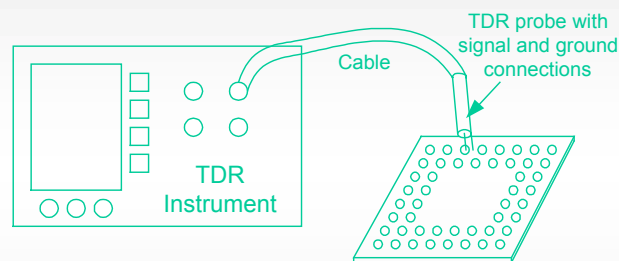
Application note: “Electronic Package Failure Analysis Using TDR”

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IConnect Failure Analysis

TDR as a Failure Analysis Technique



- **Similarities with SAM and X-ray:**
 - Sends incident signal at the DUT
 - Analyzes the reflection from the DUT

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IConnect Failure Analysis

TDR Differences from SAM and X-Ray

	TDR	SAM	X-ray
Stimulus type	Electrical	Acoustic	X-ray
Stimulus delivery medium	Electrical wires	Water	Air
Direct contact required?	Yes, signal and ground	No	No
Output presented for analysis	Package trace reflection profile	Optical image	Optical image
Ability to locate failures between package layers	Good	Poor	Poor

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IConnect Failure Analysis

Opens and Shorts: IConnect FA Methods

- **Signature analysis**
- **Comparative analysis**
- **Physical vs. Electrical Length Analysis**
- **Layer correlation analysis**

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IConnect Failure Analysis

Signature Analysis: TDR and Impedance Profile

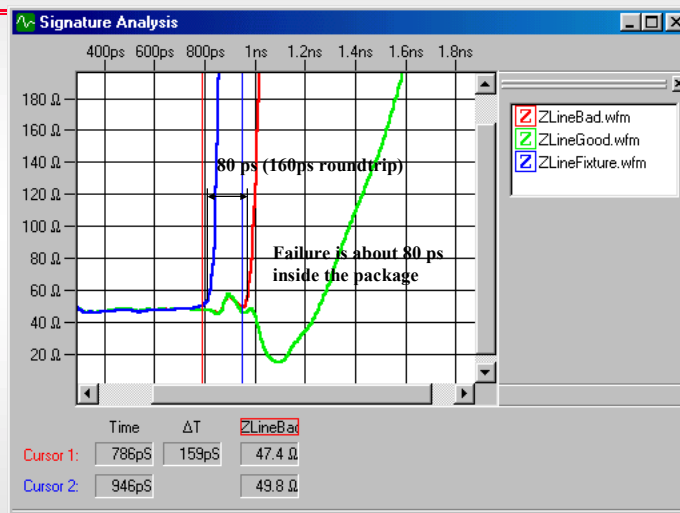


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IConnect Open Failure Analysis

Open Signature Analysis

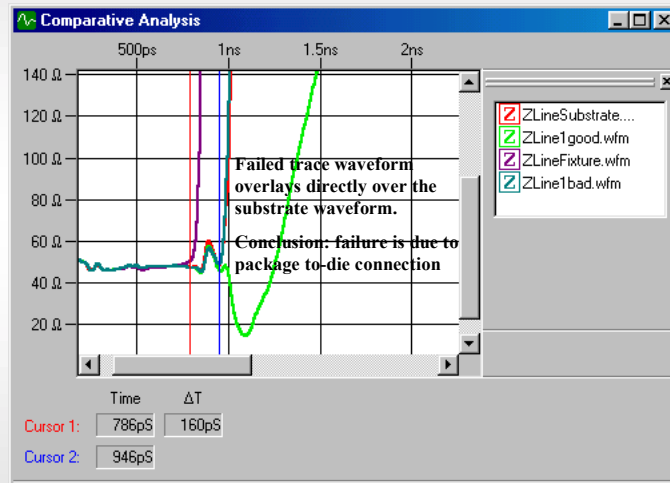


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IConnect Open Failure Analysis

Open Comparative Analysis

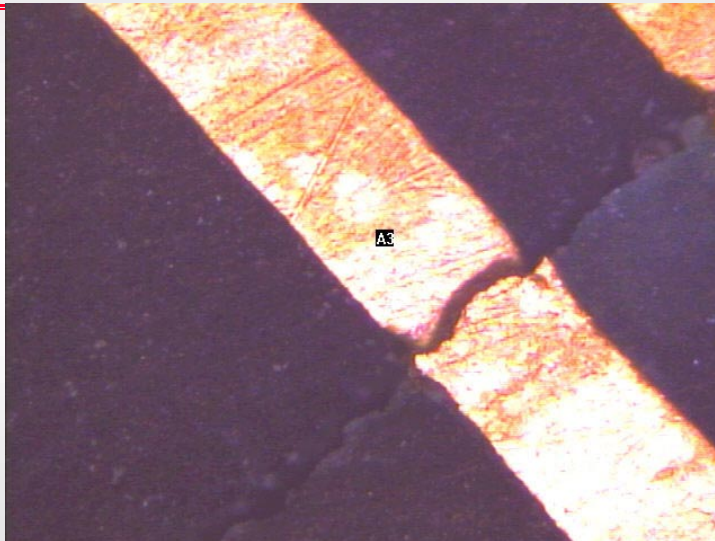


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Physical Analysis, Parallel Lapping

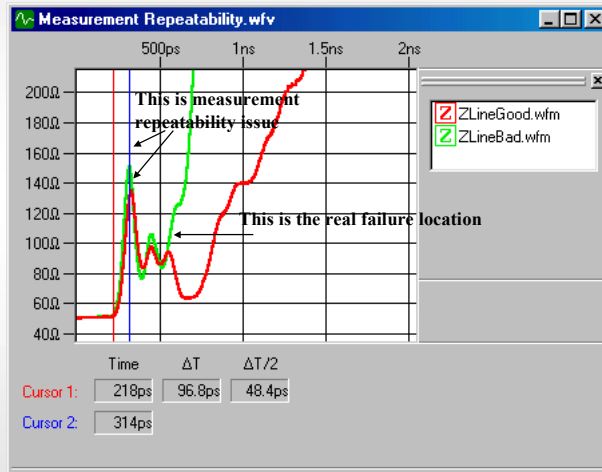


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IConnect Open Failure Analysis

TDR Measurement Repeatability

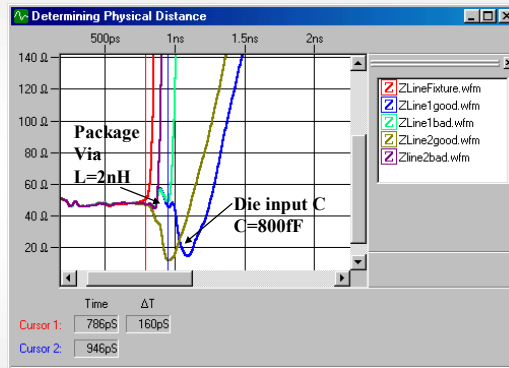
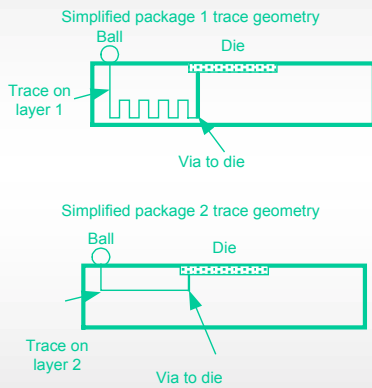


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IConnect Open Failure Analysis

Open Correlation Analysis



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ICConnect Open Failure Analysis

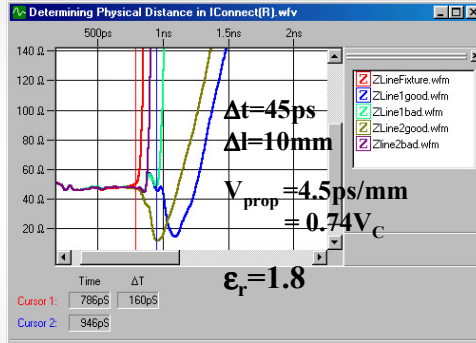
Physical vs. Electrical Length Analysis

$$\frac{V_{prop\ average}}{V_C} = \frac{I_{total}}{t_{d\ total}} \cdot \frac{1}{V_C}$$

$$I = t_d \cdot \frac{I_{total}}{t_{d\ total}}$$

ICConnect uses ϵ_r

$$\epsilon_r\ average = \left(\frac{V_C}{V_{prop\ average}} \right)^2 = \left(\frac{V_C \cdot t_{d\ total}}{I_{total}} \right)^2$$

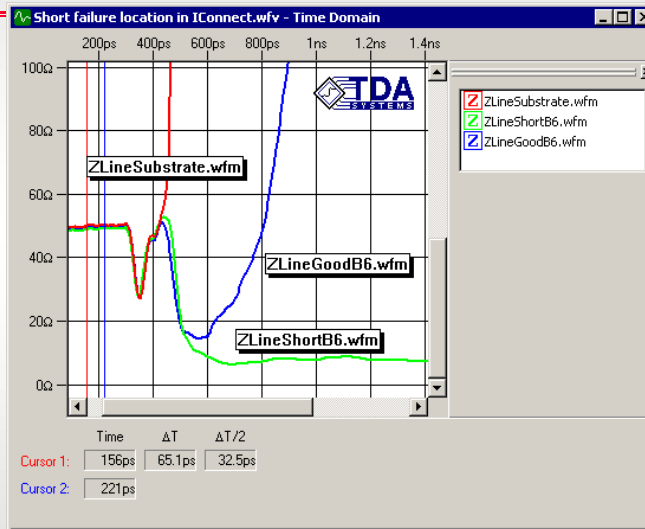


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ICConnect Short Failure Analysis

Short Failure Analysis



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IConnect Short Failure Analysis

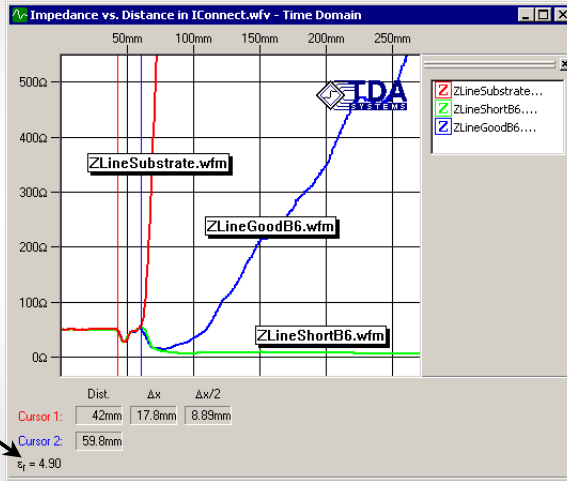
Short Failure: Impedance vs. Distance

$$\Delta t = 63 \text{ ps}$$

$$\Delta l = 8.7 \text{ mm}$$

$$V_{\text{prop}} = 7.24 \text{ ps/mm}$$

$$\epsilon_r = 4.9$$

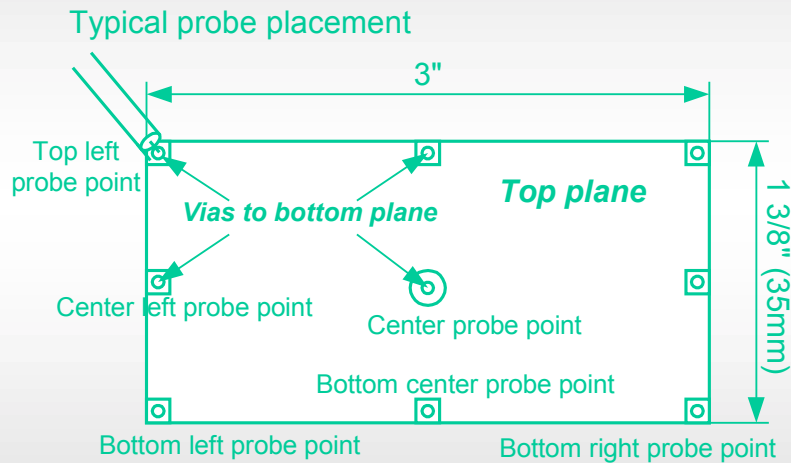


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IConnect Short Failure Analysis

Plane-to-Plane Shorts: Test Vehicle (TV)

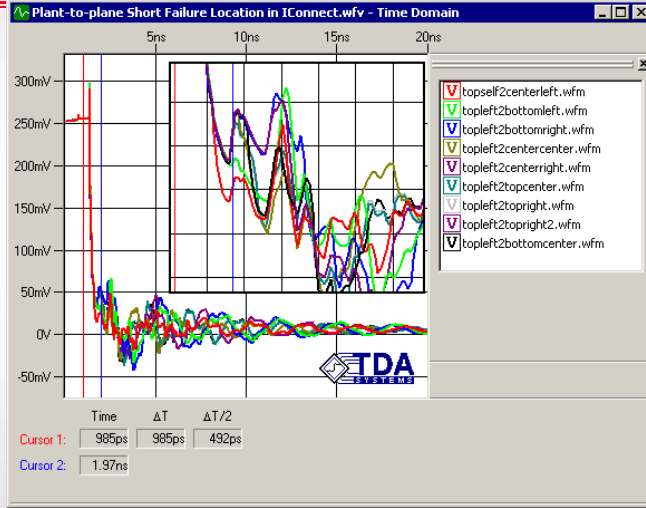


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ICConnect Short Failure Analysis

Plane-to-Plane Short TV Measurement

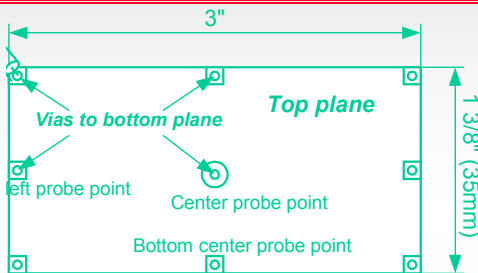


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ICConnect Short Failure Analysis

Plane-to-Plane Shorts TV Results



Physical expectations			
	Left	Center	Right
Top	X	2	6
Center	1	4	7
Bottom	3	5	8

Electrical length results			
	Left	Center	Right
Top	X	4	5
Center	1	3	7
Bottom	2	6	8

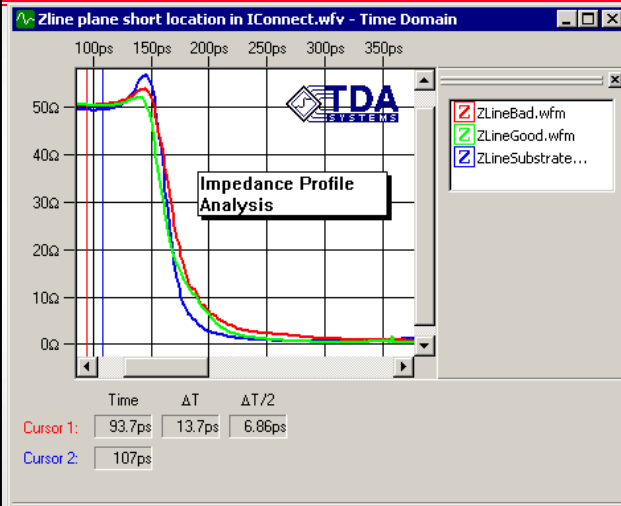
Inductance results			
	Left	Center	Right
Top	X	3	4
Center	1	5	7
Bottom	6	2	8

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ICConnect Short Failure Analysis

Plane-to-Plane Shorts: Actual Package



- 1 – Substrate
- 2 – Good die
- 3 – Bad (failing) DUT

Substrate – 400 pH

Good die – 600 pH

Bad (failing) DUT – 800pH

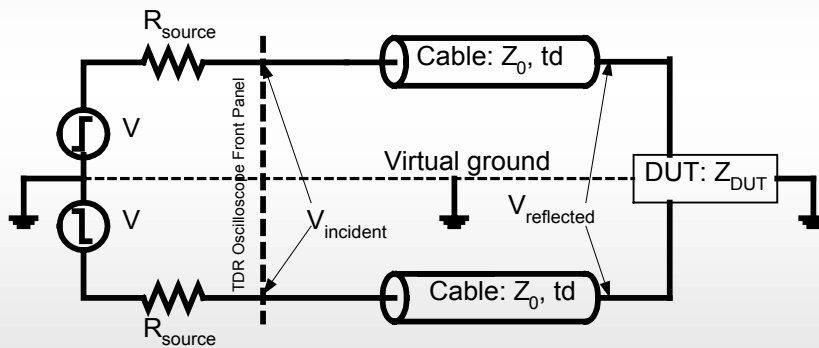
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ICConnect Failure Analysis

Signal to Signal or Plane to Plane Shorts

- Try differential TDR!



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Collateral

- **Presentation Handouts**
www.tdasystems.com/training.htm
- **Application materials**
www.tdasystems.com/support.htm
- **TDR References**
www.tdasystems.com/bibliography.htm

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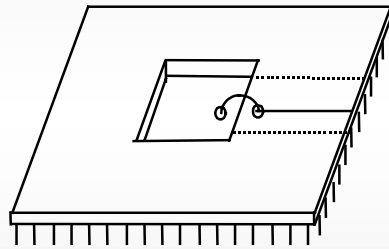
Outline

- ✓ **TDR Impedance Measurements**
- ✓ **Interconnect Failure Analysis**
- ✓ **Interconnect Signal Integrity Modeling**
- **Discussion and practical session**

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Supplementary Information



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Transmission line equation reference

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \approx \sqrt{\frac{L}{C}}$$

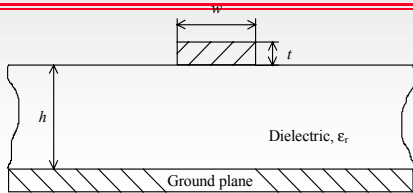
$$V_p = \frac{1}{\sqrt{LC}}$$

$$L = Z_0 \cdot t_p \quad C = \frac{t_p}{Z_0}$$

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Basic Stripline and Microstrip Equations

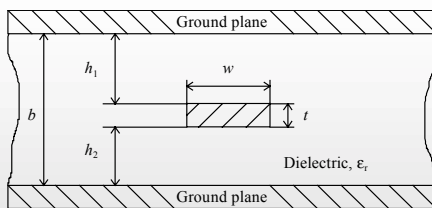


$$Z_0 = \frac{87}{\sqrt{\epsilon_r + 1.41}} \cdot \ln\left(\frac{5.98 \cdot h}{0.8 \cdot w + t}\right)$$

$$V_p = 1.017 \cdot \sqrt{0.475 \cdot \epsilon_r + 0.67} \quad \text{ns/ft}$$

for $0.1 < w/h < 2.0$

$1 < \epsilon_r < 15$



$$Z_0 = \frac{60}{\sqrt{\epsilon_r}} \cdot \ln\left(\frac{4 \cdot b}{0.67 \cdot \pi \cdot (0.8 \cdot w + t)}\right)$$

$$V_p = 1.017 \cdot \sqrt{\epsilon_r} \quad \text{ns/ft}$$

for $w/b < 3.5$

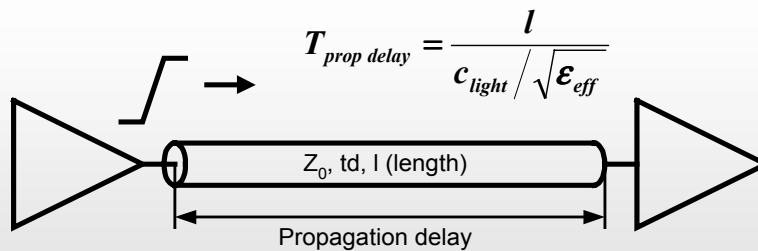
$t/b < 0.25$

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Propagation Delay

- Time required for signal to propagate through interconnect
- Dependent on velocity and interconnect length
- Examples:
 - prop. delay in vacuum: $1/c_{\text{light}} = 1 \text{ ns/foot}$ (velocity $3 \cdot 10^8 \text{ m/sec}$)
 - propagation delay per length in FR4: 150 ps/inch



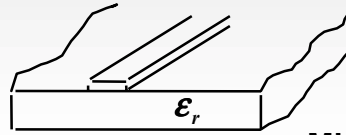
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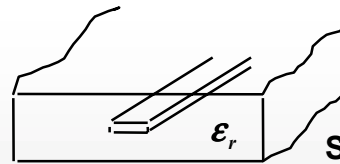
Propagation Delay in Transmission Lines

$$T_{prop\ delay} = \frac{l}{c_{light} / \sqrt{\epsilon_{eff}}} = l \cdot \sqrt{LC}$$

- c_{light} is speed of light in vacuum ($3 \cdot 10^8$ m/sec)
- ϵ_{eff} depends on ϵ_r of the board material
 - and ϵ_r of air for microstrip
- L, C are inductance and capacitance per unit length



Microstrip



Stripline

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Can You Ignore Propagation Delay?



- Practical rule of “short interconnect”

$$t_{rise} > t_{prop\ delay} \cdot 6$$

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Interconnect vs. IC Propagation Delay

- IC propagation delay decreases as the IC technology improves
- Interconnect delay depends only on the length and board material
 - unless ϵ_{eff} or length decrease, interconnect delays will stay constant

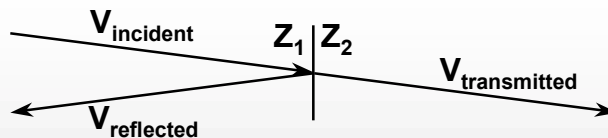
$$T_{prop\ delay} = \frac{l}{c_{light} / \sqrt{\epsilon_{eff}}}$$

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Reflections in Interconnects

- Interconnects are transmission lines
- Impedance is the measure of *transmission properties* of interconnects
- In *any transmission media*, at the impedance discontinuity part of the energy is reflected back

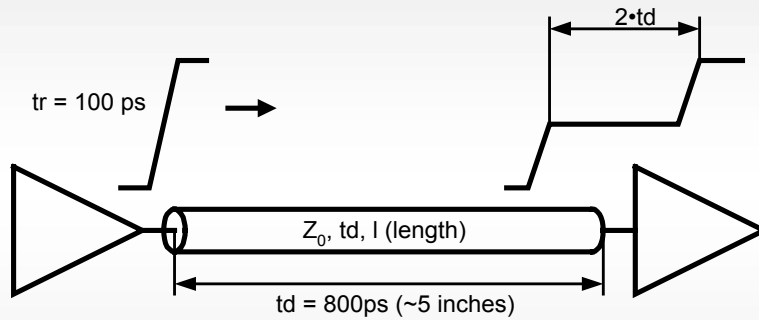


Reflection coefficient: $\Gamma = \frac{V_{reflected}}{V_{incident}} = \frac{Z_2 - Z_1}{Z_2 + Z_1}$

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Reflections Example: Long Interconnect

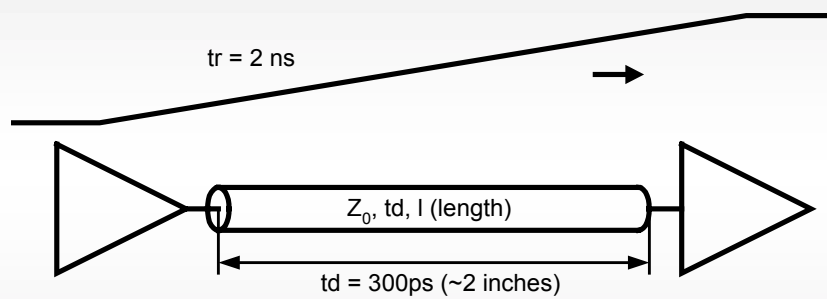


- Digital threshold switching and timing errors are likely

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Reflections Example: Short Interconnect

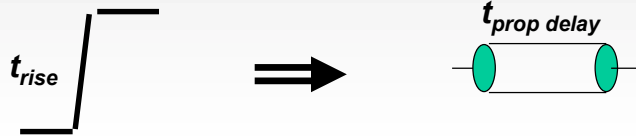


- Rarely a problem

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Can You Ignore Reflections?



- Practical rule of “short interconnect”

$$t_{rise} > t_{prop\ delay} \cdot 6$$

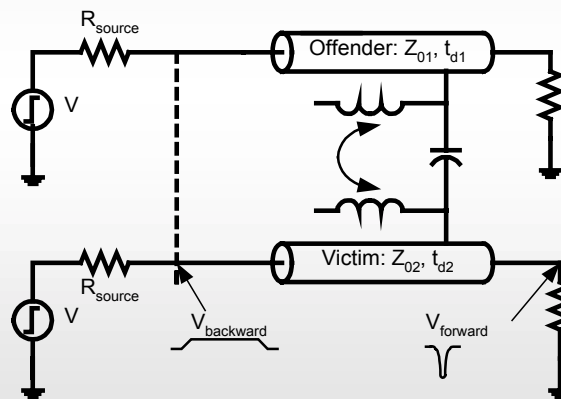
- Ringing still may occur due to discontinuities (RLC)

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Crosstalk

- Energy coupling between adjacent lines
- Forward (far-end) and backward (near-end)
- Sum of capacitive and inductive



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Forward and Backward Crosstalk

- **Forward crosstalk (near end of the victim)**
 - proportional to rise time of the signal on offender
 - proportional to the line length
 - positive for capacitive and negative for inductive
 - near zero for stripline

$$K_f = \text{forward crosstalk constant} = -\frac{1}{2} \cdot \left(\frac{L_m}{Z_0} - C_m \cdot Z_0 \right)$$

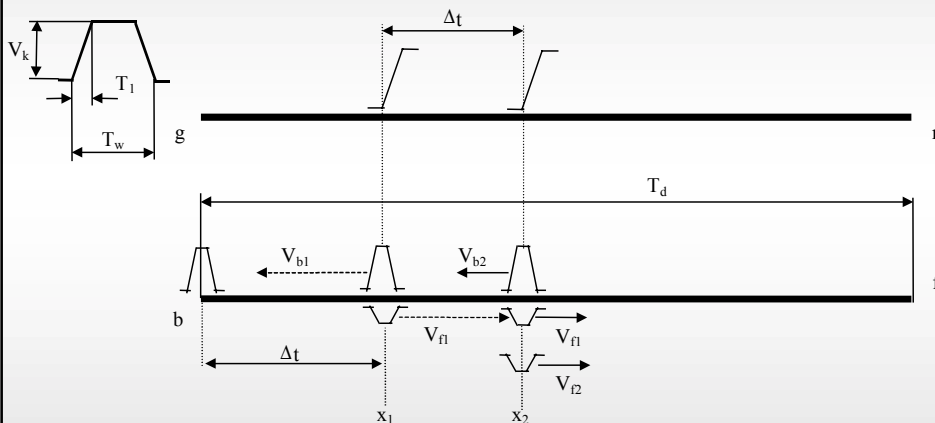
- **Backward Crosstalk**
 - not a function of rise time
 - sum of capacitive and inductive

$$K_b = \text{backward crosstalk constant} = \frac{l}{4 \cdot T_{prop\ delay}} \cdot \left(\frac{L_m}{Z_0} + C_m \cdot Z_0 \right)$$

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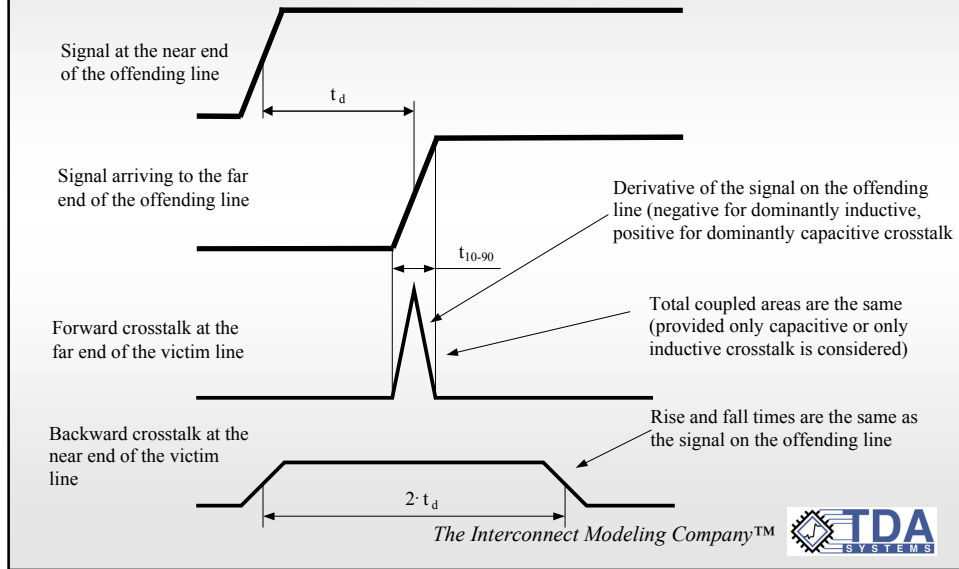
Crosstalk Formation



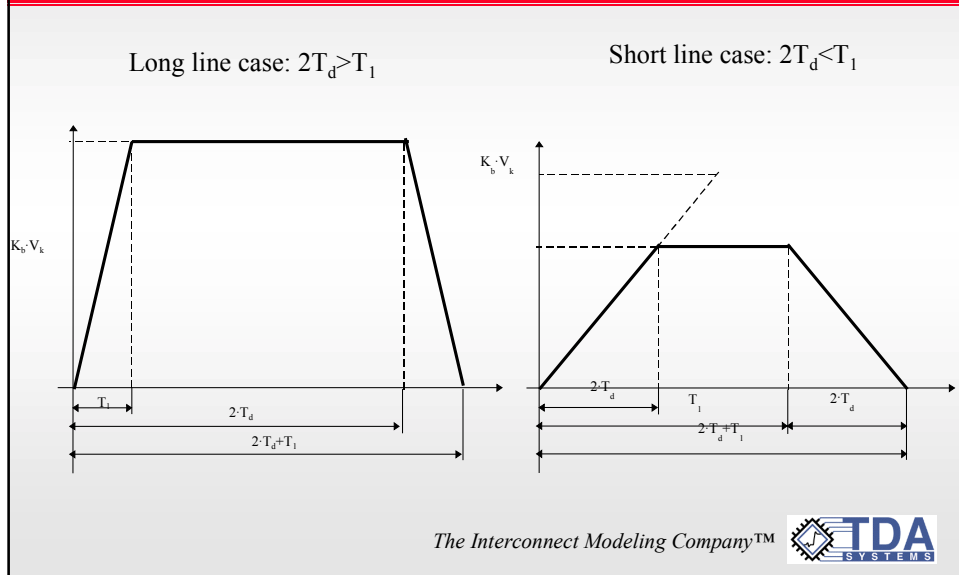
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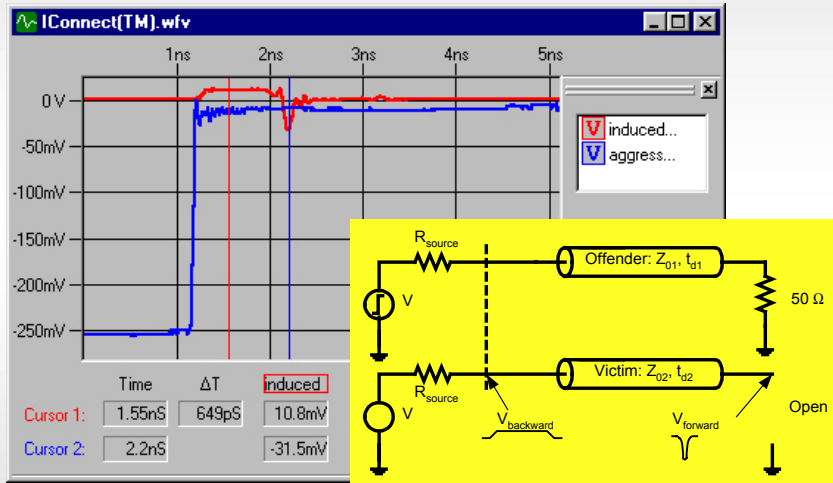
Crosstalk Observations



Backward crosstalk for short and long line



Crosstalk Example



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Losses

- Skin effect losses

$$R_s = \frac{g}{P} \sqrt{\frac{\pi \cdot \mu}{\sigma}} \cdot \sqrt{f} \quad \Omega/\text{inch}$$

Example (copper):

$$R = \frac{g}{P} \cdot 3.07 \cdot 10^{-7} \cdot \sqrt{f} \quad \Omega/\text{inch}$$

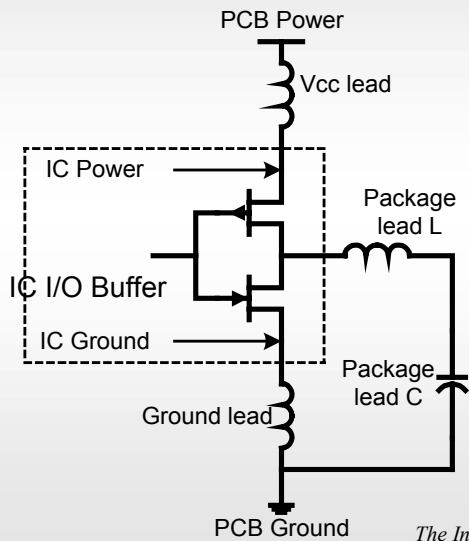
- Dielectric Losses

$$G = g_d \cdot 2 \cdot \pi \cdot f \cdot \epsilon \cdot \tan \delta$$

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Ground Bounce, or Simultaneous Switching Noise (SSN)



- **SSN cause: inductance between IC, package and PCB ground**
- **SSN factors:**
 - signal rise time
 - number of simultaneously switching buffers
 - package inductance
 - load capacitance

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Rise Time Degradation

$$t_{\text{interconnect}} = \frac{0.35}{BW_{\text{interconnect}}}$$

$$t_{r \text{ final}} = \sqrt{t_{\text{signal}}^2 + t_{\text{interconnect}}^2}$$

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Dispersion

- Signal integrity degradation due to pulse dispersion
- Typically not present strongly in megahertz signals



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