ECE1371 Term Paper
RF Receiver Systems and Circuits
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I. Introduction

In the past decade, portable wireless communication systems have experienced tremendous growth. Such rapid growth has created demand for portable wireless devices that are smaller, lighter, cheaper and of higher performance than ever, and this drives IC designers and engineers to innovate new system architectures and circuit topologies. One goal is to build RF receiver IC's that has low power consumption, high sensitivity and wide dynamic range, and to reduce the number of off-chip passive components in the circuit. This paper therefore focuses on the receiver portion of a wireless device, providing a review of conventional receiver architectures as well as some of the latest research in RF receiver IC's is provided. The conclusion at the end of the paper also discusses the trend in future RF receiver design.

II. Receiver Architectures

This section describes three common receiver architectures: heterodyne, homodyne and image-reject, all of which have different advantages and drawbacks. When designing a RF receiver, the choice of architecture is primarily determined by criteria including complexity, cost, power dissipation and the number of external components [1]. Heterodyne is the architecture that was selected for most of the cellular handsets in the past [2], but as IC process and technology evolve, other approaches, such as homodyne, have also become a plausible solution to some of the design problems [1].

A. Heterodyne Receivers

A simplified block diagram of a heterodyne receiver is shown in figure 1. The incoming RF signal from the antenna is first filtered by a band select filter that removes the out-of-band signals. It is then amplified by a low noise amplifier (LNA), which also suppresses the contribution of the noise from the succeeding stages. The LNA output is then filtered by an image-reject filter to remove the image, which has an offset of twice the intermediate frequency from the desired channel signal, before being down-converted to the intermediate frequency (IF) by the mixer. A channel-select filter then performs channel selection at the IF, and after that demodulation or detection is carried out to retrieve the desired information.
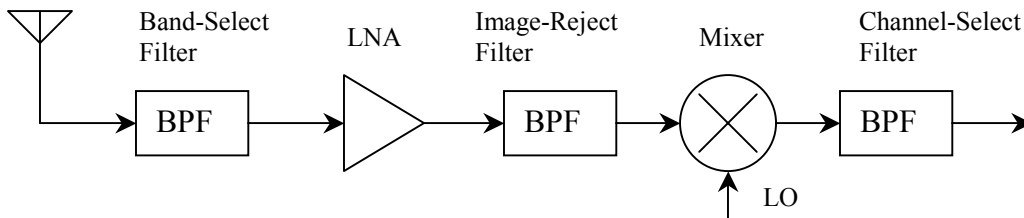

Figure 1. Simplified Block Diagram of Heterodyne Architecture

This single-IF scheme can lead to severe trade-off between sensitivity and selectivity [1]. If the intermediate frequency is high, the image then appears far away from the desired signal band and can easily be suppressed by a bandpass filter with typical cutoff characteristics. However, the channel selection filter now requires a very high Q-factor, which is defined as the ratio of the center frequency to the 3dB bandwidth, and filters with very high Q are difficult to design. If the IF is low, the channel selection has a more relaxed requirement, but proper image suppression becomes harder to achieve. Figure 2 shows the problems for high and low IF.
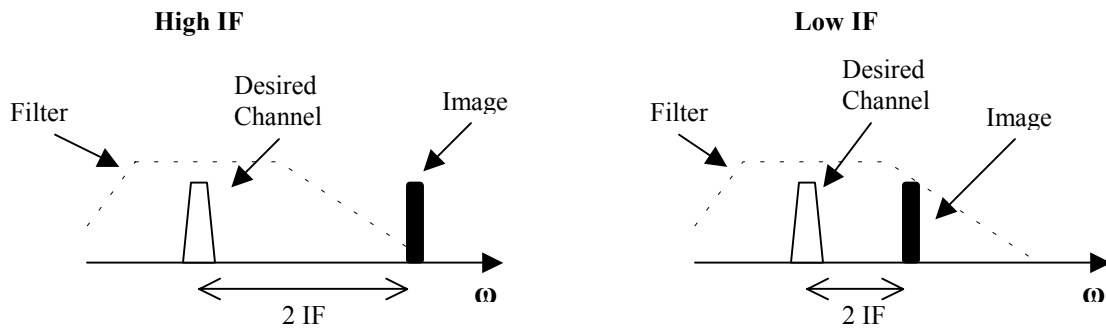
Figure 2. Effect of Image for High and Low IF

In practice, more than one IF mixer stage can be used to alleviate the conflict between sensitivity and selectivity. For example, in a dual-IF heterodyne receiver, the RF signal is first down-converted to an IF that is high enough to allow easy suppression of the image. It is then down-converted to a second IF that is much lower than the first one to ease channel selection [1].

B. Homodyne Receivers

In a homodyne or direct conversion receiver, the incoming RF signal is down-converted to baseband (zero frequency) in one step by mixing with an oscillator output of the same frequency. The resulting baseband signal is then filtered with a low-pass filter to select the desired channel. This is illustrated in the block diagram in figure 3.
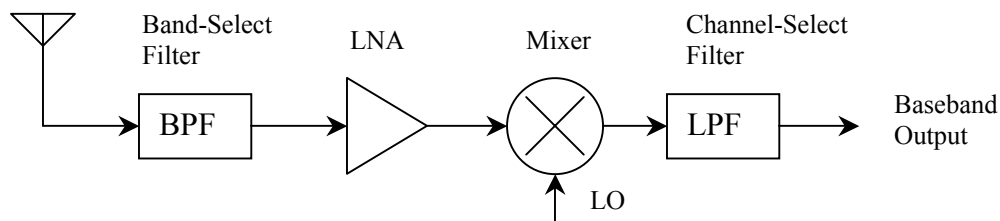

Figure 3. Simplified Block Diagram of Homodyne Architecture

The main advantage of a homodyne receiver is that it does not suffer the image problem as the incoming RF signal is down-converted directly to baseband without any IF stage. Another advantage of the homodyne architecture is its simplicity. Since it does not require any high frequency band-pass filter, which are usually implemented off-chip in a super-heterodyne receiver for appropriate selectivity [2], the homodyne requires less number of external components. However, the homodyne architecture does suffer from a number of implementation issues. The major disadvantage is that severe DC offsets can be generated at the output of the mixer when the leakage from the local oscillator is mixed with the local oscillator signal itself. This could saturate the following stages and affect the signal detection process. Also, since the mixer output is a baseband signal, it can easily be corrupted by the large flicker noise of the mixer [3], especially when the incoming RF signal is weak.

C. Image-Reject Receivers

Although the image in a heterodyne receiver can be suppressed by filtering the signal with an image-reject filter, the image-reject filter has to operate at RF and the cutoff of the filter must be sharp, especially in systems having a low IF. This imposes a strict requirement on the Q-factor of the image-reject filter, as mentioned previously. In order to ease the design of the receiver while providing image-rejection, the image-reject architectures can be used.
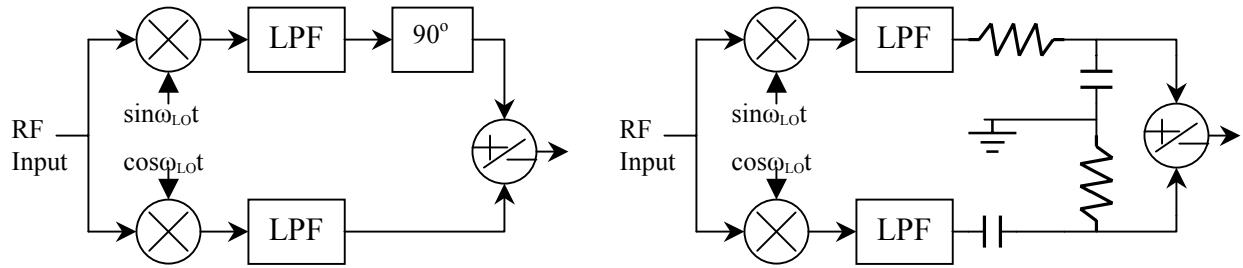
Figure 4 (a) Harley Architecture (b) Typical Implementation

One type of image-reject receiver is the Hartley architecture [1]. The block diagram is shown in figure 4(a). The RF signal is first mixed with quadrature phases of the local oscillator signal. After filtering both mixer output with a low-pass filter, one of the resulting signals is shifted by 90°. Therefore, the sum of the two final signals cancels the image band to yield the desired signal, while the subtraction removes the desired band and selects the image. The main drawback of this architecture is that the receiver is very sensitive to the phase errors of the local oscillator signals [1], which causes incomplete image cancellation. Also, in the typical implementation of the Hartley architecture as shown in figure 4(b), mismatches of the R and C in the two signal paths due to process variations affect the image cancellation process.

Another type of image-reject receiver is the Weaver architecture (figure 5). It is very similar to the Harley architecture, except that the 90° phase shift in one of the signal paths is replaced by another set of mixing operation in both signal paths. Similar to the Hartley receiver, if the phase difference of the two local oscillator signals is not perfectly 90°, the image can no longer be cancelled completely.
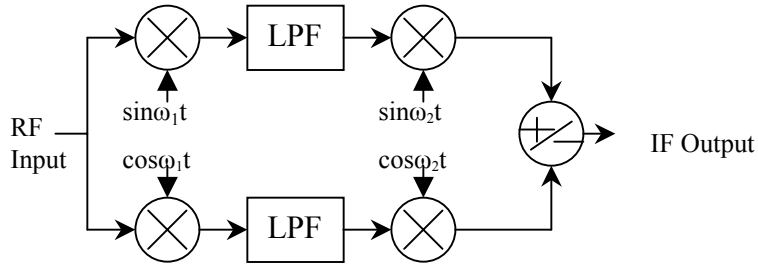
Figure 5. Simplified Block Diagram of the Weaver Architecture

III. Receiver Performance Characterization

To understand the design choices made in RF receiver systems, some standard parameters must be utilized to evaluate the performance of the receiver in the corresponding application. Apart from power dissipation which is important for all integrated circuits, an RF receiver is characterized by its sensitivity and dynamic range.

One parameter that describes the sensitivity of a receiver is the minimum detectable signal (mds). It is related to the receiver noise and the system bandwidth by [1]:

$$\text{mds (dBm)} = -174 \text{ dBm} + 10 \log \text{BW} + \text{NF} + \text{SNR}$$

where BW is the overall system bandwidth. NF is the receiver noise figure, which is defined as the ratio of the total noise to the noise contributed by the source, all referred to the output. SNR is the signal-to-noise ratio required at the demodulator or detector input to achieve an acceptable bit-error rate, which is typically 10^{-3} [4].
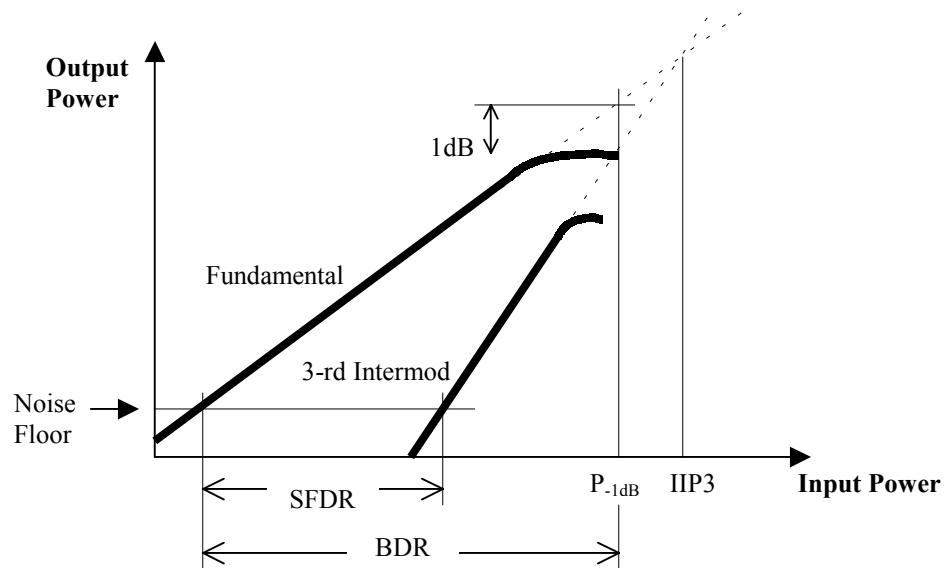
Figure 6. Definitions of Dynamic Range Parameters

Regarding the dynamic range of a receiver, two definitions can be applied: spurious-free dynamic range (SFDR) and blocking dynamic range (BDR) [4] (figure 6). SFDR is the input signal range from the noise floor up to the input power that creates intermodulation products equal to the noise power, while BDR is the input power range from the noise floor up to the 1-dB gain compression point (P_{-1dB}) [4]. Intermodulation products are undesired harmonics arising from the non-linearity of the receiver components [5], including the LNA and the mixers. In most RF receivers, third-order intermodulation dominates and the corresponding distortion is specified by the third-order intercept point (IP3), which is the intersection point of the fundamental frequency component gain curve and the third-order harmonics gain curve (see figure 6). In homodyne systems, even-order distortion can be severe [1] and the second-order intercept point (IP2) is also specified. The 1-dB gain compression point is the input power which compresses the linear gain (fundamental frequency component) by 1dB. The above parameters can be related to each other by the following relationships [4]:

$$P_{-1dB} = IIP3 - 9.64 \text{ dB}$$

$$\text{Noise Floor} = -174\text{dBm/Hz} + NF + 10 \log BW$$

$$SFDR = \frac{2}{3}(IIP3 - \text{Noise Floor})$$

$$BDR = P_{-1dB} - \text{Noise Floor}$$

The overall receiver dynamic range can therefore be determined by the noise figure and intermodulation intercept point of each individual component. For example, the cascaded noise figure and the cascaded intercept point of a system with three cascaded stages (figure 7) can be calculated by the following two equations [4,5]:

$$NF_{TOTAL} = NF_1 + \frac{1}{A_{V1}}(NF_2-1) + \frac{1}{A_{V1}A_{V2}}(NF_3-1)$$

$$IIP3_{TOTAL} = [\ \frac{1}{IIP3_1} + \frac{A_{V1}}{IIP3_2} + \frac{(A_{V1}A_{V2})^2}{IIP3_3}\ ]^{-1}$$

where A_{Vi} is the gain of stage i, NF_i the noise figure of stage i, and $IIP3_i$ the 3-rd order intercept point of stage i.

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     Stage 1              Stage 2              Stage 3
 ┌──────────────┐    ┌──────────────┐    ┌──────────────┐
→│ Gain = A_V1  │→  →│ Gain = A_V2  │→  →│ Gain = A_V3  │→   NF_TOTAL
 │ NF_1, IIP3_1 │    │ NF_2, IIP3_2 │    │ NF_3, IIP3_3 │    IIP3_TOTAL
 └──────────────┘    └──────────────┘    └──────────────┘
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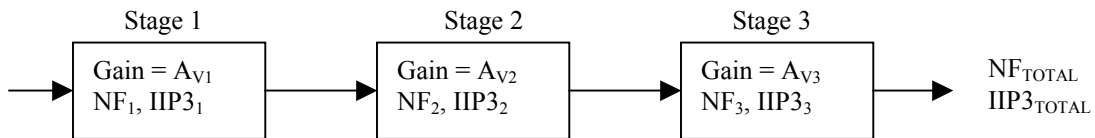
Figure 7. System with Three Cascaded Stages

IV. RF Receiver IC's

As mentioned previously, most cellular radios in the past used the heterodyne architecture. In spite of its simplicity, the homodyne architecture was seldom used mainly

due to the dc offset problem. Since the performance and functionality requirements for many new emerging applications are different from the ones in the past, the homodyne architecture and some other approaches are becoming more practical to implement. In this section, four different RF receiver IC examples from recently published journal papers are discussed. The first three are examples of homodyne receivers, while the last one makes use of the image-reject architecture.

The first example is a frequency-hopped spread-spectrum receiver operating in the 902-928 MHz industrial, scientific and medical (ISM) band [4]. It uses the direct-conversion (homodyne) architecture as shown in figure 8(a). The incoming RF signal from the antenna is first coupled to a fully differential LNA through a transformer (with balanced load - balun). The LNA uses a common-gate topology which can be easily designed to match the 50 Ohms source impedance, the standard impedance for many RF off-chip components. The LNA consists of on-chip inductor loads as shown in figure 8(b). One of the advantages of homodyne receiver is that the off-chip image-reject filter can be eliminated; therefore, the LNA only needs to drive a capacitive load and output impedance is not required to match to a 50Ohm load. The LNA output is then down-converted to baseband and dehopped by two mixers. The channel-select low-pass filters are realized by switched-capacitor circuits operating at 14.3 MHz, and each limiter consist of an input stage, a cascade of seven differential pairs, and rectifiers to generate the received signal-strength indicator (RSSI) output as shown in figure 8(c). DC offset as large as 1V generated by self-mixing can be suppressed by the feedback loop around the limiting amplifier. The low-pass filter in the feedback loop measures the average value of

the differential limited output, and the input stage subtracts this off from the SC filter output. Since this receiver is designed for 4-FSK modulation and the baseband spectrum has relatively small enery at dc, the dc offset suppression does not affect the 4-FSK detection. This receiver is reported in [4] to have a cascaded noise figure of 8.6dB, and a cascaded IIP3 of −8.3dBm. It consumes 120mA of current from a 3V power supply.
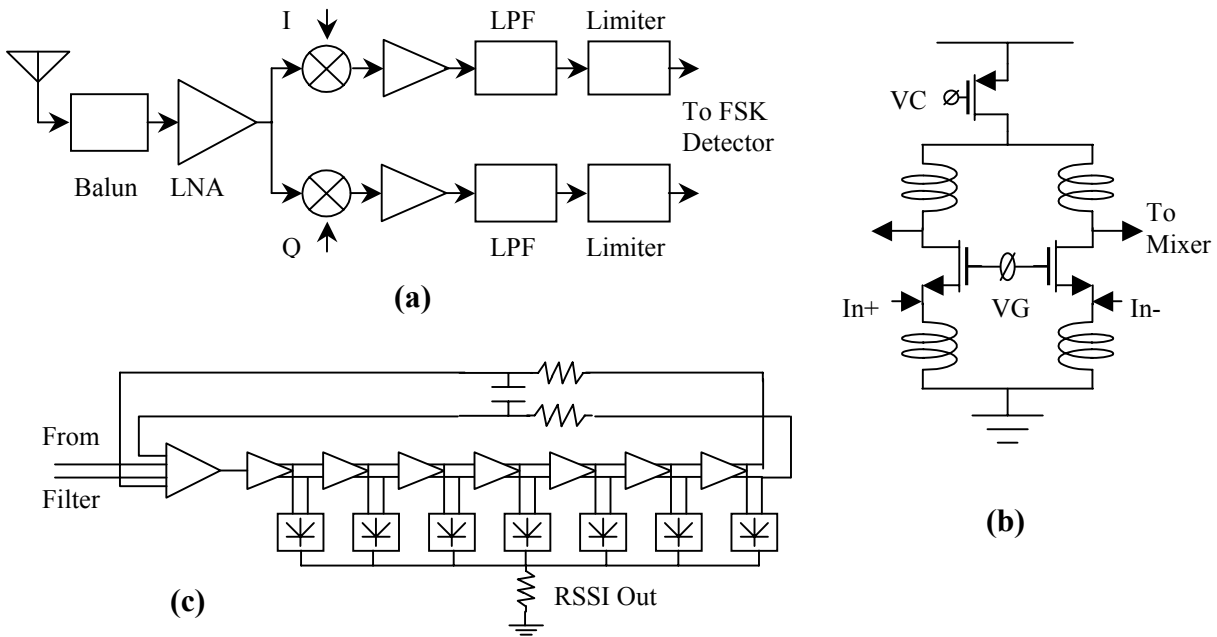

Figure 8 (a) Receiver Architecture used in [4] (b) LNA in [4] (c) Limiter in [4]

The second example is a 2-GHz wide-band receiver for WCDMA applications [6]. It is a direct-conversion receiver and the the block diagram is shown in figure 9. Unlike modulation schemes such as binary frequency shift keying, dc notch is not available in WCDMA cellular systems. However, such a wide-band spread-spectrum system is not very sensitive to removal of the dc component, because the loss of one information bit is only an average over a period due to the spreading operation with a pseudorandom sequence. The cancellation of the dc offset is therefore carried out with a

servo feedback loop around the entire baseband circuit, as shown in figure 9. According to [6], the double-sideband noise figure is 5.1dB, and the IIP3 and IIP2 are –9.5dBm and +38dBm. The receiver takes 128mA of current from a 2.7V supply.
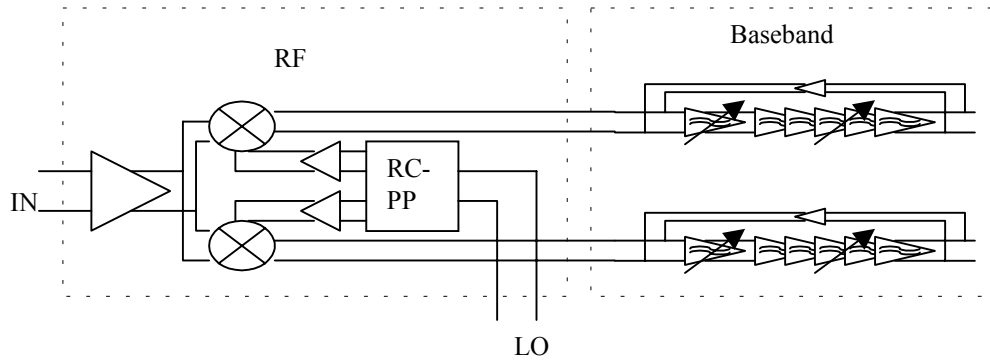

Figure 9. Architecture of 2-GHz WCDMA Receiver in [6]

The third example is taken from [7] and is a CMOS direct-conversion receiver operating in the 5.2-5.7GHz band for wireless LAN applications. Fully differential circuit topology is used throughout the entire receiver to minimize the undesired signal coupling of the local oscillator leakage, and the circuit blocks are also designed to give a high degree of isolation from the local oscillator leakge. The receiver block diagram is shown in figure 10(a).
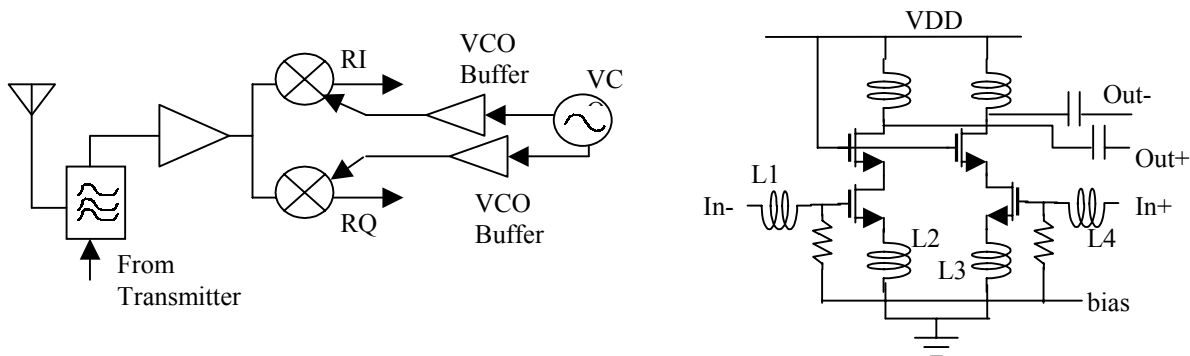

Figure 10. (a) Architecture Block Diagram of Receiver in [7] (b) LNA in [7]

The incoming RF signal is first filtered by a bandpass filter and amplified by the LNA. The LNA is a common-source amplifier as shown in figure 10(b). The input matching at each LNA input terminal is achieved by on-chip inductors L1, L2, L3 and L4. Also, the two cascode transistors are used to isolate the local oscillator leakage from the mixer back to the input, and this helps to reduce the dc offset problem. The LNA output is then down-converted to baseband by a set of mixers with quadrature signals generated by an on-chip VCO. The VCO buffers improve the isolation between the mixer and the VCO, and provide large local oscillator signal which can increase mixer linearity and noise performance. As reported in [7], the receiver has a double-sideband noise figure of 3dB, an input 1-dB compression point of −21dBm, an IIP2 of 16.1dBm, an IIP3 of −11.3dBm and a power dissipation of 114mW at 3V power supply.

The last example is a CMOS receiver for Dual-Band Applications [8]. It employs the Weaver image-reject architecture and operates in the 900-MHz/1.8-GHz band. Figure 11 shows the block diagram of the receiver. It takes advantage of the fact that addition and subraction of the image-reject receiver output can select the signal band located an IF above or below the local oscillator frequency (see figure 11). Two separate sets of duplexer, LNA's and first IF mixers are used for the two signal bands. The band-select control shuts off the path that is idle to save power comsumption. The output from the first IF mixers are then filtered by the two bandpass filters, and a second set of mixers produce the I and Q basband output. The band-select control then selects the desired band by choosing either addition or subtraction. Since the first IF is midway between 900-MHz and 1.8-GHz, the 900-MHz spacing between the image and the desired signal band allows

substantial supression of the image in the duplexers [8]. The reported receiver noise figure and IIP3 at 900-MHz is 4.7dB and −8dBm, and 4.9dB and −6dBm at 1.8-GHz. The total power dissipation is 75mW with a 3V power supply.
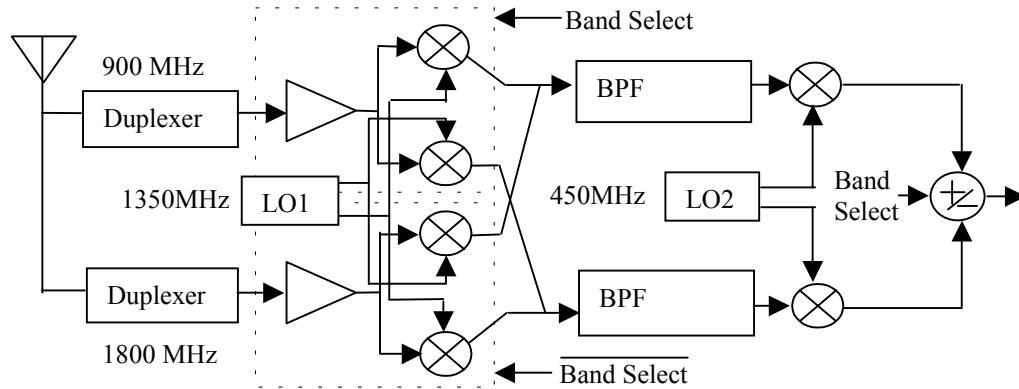

Figure 11. Dual-band Receiver Architecture in [8]

V. Future RF Receivers

With the introduction of new wireless standards such as Bluetooth and third-generation cellular standard, future RF receivers need to process not only voice but also data signal at a comparatively high bit rate. This creates many challenges to RF receiver design because the receivers must be more compact with superior performance in order to satisfy the requirements of these new applications. It is also desirable to integrate multi-standard functionality on a single chip, and this means an even higher level of electronics integration is required to build these multi-standard multi-band receivers in a cost-effective manner. As seen from the foregoing discussions and examples of RF receiver IC's, much work is being done to minimize the number of off-chip components and chip area, and innovations in new receiver architectures and circuit topologies are being made to accomplish these goals.

References

[1] B. Razavi, *RF Microelectronics*, Prentice-Hall, Upper Saddle River, 1998.

[2] S. Mattisson, *Technology Directions In Cellular Receivers*, n.d.

[3] H. Darabi, A. Abidi, "A 4.5mW 900-MHz CMOS Receiver for Wireless Paging", *IEEE Journal of Solid-State Circuits*, vol. 35, pp. 1085-1096, Aug. 2000

[4] A. Rofougaran, G. Chang, J. Rael, J. Chang, M. Rofougaran, P. Chang, M. Djafari, J. Min, E. Roth, A. Abidi, H. Samueli, "A Single-Chip 900-MHz Spread-Spectrum Wireless Transceiver in 1-um CMOS - Part II: Receiver Design", *IEEE Journal of Solid-State Circuits*, vol 33, pp. 535-547, Apr. 1998.

[5] D. Pozar, *Microwave Engineering*, John Wiley & Sons, 1997

[6] A. Parssinen, J. Jussila, J. Ryynanen, L. Sumanen, K. Halonen, "A 2-GHz Wide-Band Direct Conversion Receiver for WCDMA Applications", *IEEE Journal of Solid-State Circuits*, vol 34, pp. 1893-1903, Dec 1999.

[7] T. Liu, E. Westerwick, "5-GHz CMOS Radio Transceiver Front-End Chipset", *IEEE Journal of Solid-State Circuits*, vol 35, pp. 1927-1933, Dec. 2000.

[8] S. Wu, B. Razavi, "A 900-MHz/1.8-GHz CMOS Receiver for Dual-Band Applications", *IEEE Journal of Solid-State Circuits*, vol 33, pp. 2178-2185, Dec. 1998.